

# Quantum Inspire Starmon-5 Fact Sheet

G.R. Di Carlo and L. DiCarlo

QuTech and Kavli Institute of Nanoscience, Delft University of Technology, P.O. Box 5046, 2600 GA Delft, The Netherlands (Dated: March 16, 2024)

> This fact sheet provides further information on the Starmon-5 superconducting backend of Quantum Inspire, including the quantum processor layout, cryogenic wiring, control electronics, quantum operations, and reported metrics.

### I. QUANTUM PROCESSOR

Starmon-5 is a superconducting quantum processor based on circuit quantum electrodynamics [1, 2]. It consists of five transmon qubits [3] in an X-shaped coupling configuration. A schematic of the 8 mm × 8 mm chip is shown in Fig. 1. Dedicated bus resonators connect nearest-neighbor pairs, enabling two-qubit gates between any corner transmon  $(Q_0, Q_1, Q_3, Q_4)$  and the central transmon  $(Q_2)$ . Each transmon is also connected to a microwave-control line for singlequbit gating, a flux-control line for two-qubit gating, and a dispersively-coupled resonator for readout. Every readout resonator has an accompanying Purcell filter [4]. The readout resonator structures for qubits  $Q_0, Q_2, Q_3$ , and  $Q_4$ couple to one feedline, and those for qubit  $Q_1$  to another. The unique frequencies of readout structures on the common feedline allow simultaneous, independent qubit readout by frequency multiplexing. The 7-port connectivity of these transmon qubits gives them a characteristic star shape and hence the nickname *Starmon* [5]. All inputs and outputs of the device are connected to a Cu printed circuit board using Al wirebonds, as shown in Fig. 2.



FIG. 1. Schematic diagram of the Starmon-5 quantum processor. The transmons are represented as circles, with color indicating high-frequency (red), mid-frequency (blue), and low-frequency (pink) transmons. The processor architecture follows Ref. [5].



FIG. 2. Optical image of a similar device mounted to its Cu printed circuit board.

# **II. DILUTION REFRIGERATOR WIRING**

Starmon-5 is cooled in a  ${}^{3}\text{He}/{}^{4}\text{He}$  dilution refrigerator (Leiden Cryogenics CF-650) with a base temperature of 19 mK. A detailed diagram of the wiring of readout, microwave-control, and flux-control lines inside the refrigerator is shown in Fig. 3. The status of the refrigerator can be followed in real time via this link.

#### III. CONTROL ELECTRONICS

The Starmon-5 processor is controlled using a room-temperature electronics stack. This stack combines specialpurpose QuTech-built and commercial electronics, as shown in the schematic in Fig. 3.

The QuTech Central Controller is an all-digital instrument whose primary function is to orchestrate the action of all control and readout instruments. This sequencer can generate up to 50 million sequences per instrument per second. It makes use of a distributed architecture to control up to 12 analog instruments per rack, ensuring the flexibility and extensibility of the control setup beyond Starmon-5. It achieves this while guaranteeing timing determinism.

The Zurich Instruments High-Density Arbitrary Waveform Generator (HDAWG8) is an eight-channel arbitrary waveform generator (AWG) used to produce both the flux pulses required for two-qubit gates and the envelopes of microwave-frequency pulses used for single-qubit gates. The HDAWG8 has real-time filtering capabilities that we use to correct the linear-dynamical distortions in the flux-control lines [6]. Starmon-5 makes use of 3 HDAWGs in total (one for flux control, and two for microwave control).

The Zurich Instruments Ultra-High Frequency Quantum Analyzer (UHFQA) is an all-in-one two-channel AWG and two-channel digitizer used to perform readout. The AWG produces the envelopes of microwave readout pulses injected to a feedline. The digitizer performs demodulation and weighted integration of the feedline output signal (after amplification and frequency down-conversion) and thresholds, producing a one-bit outcome for each qubit measured. Starmon-5 makes use of two UHFQAs, one per feedline.

The Zurich Instrument Super-High Frequency Parametric Pump Controller (SHFPPC) is used to provide the pump tone for each travelling-wave parametric amplifier (TWPAs), and also to interferometrically null the pump at the input to the readout down-conversion mixer.



FIG. 3. Diagram the cryogenic wiring used in Starmon-5.

### IV. QUBIT OPERATIONS

Single-qubit gates: The native single-qubit gates of Starmon-5 are I, the longitudinal gates Z,  $S S^{\dagger}$ , T, and  $T^{\dagger}$ , and the transversal gates X, X90, mX90, Y, Y90, mY90, x-axis rotations  $R_x(\theta)$ , and y-axis rotations  $R_y(\theta)$ , with  $\theta$  any multiple of  $\pi/28$ . While users can specify arbitrary  $\theta$ , the compiler quantizes it to the nearest multiple of  $\pi/28$ ). The above longitudinal gates are implemented using virtual Z gates (i.e., updating the phase of the reference oscillatorn for each qubit). The transveral gates are implemented as DRAG pulses [7, 8], with their characteristic gaussian and derivative-of-gaussian envelopes. All native single-qubit gates complete within 20 ns. This includes I, which amounts to 20 ns of idling.

Starmon-5 supports other single-qubit gates non-natively. These are:

- *H*, realized as  $R_x(\pi)R_y(\pi/2)$ ,
- $R_z(\theta)$ , realized as  $R_y(-\pi/2)R_x(\theta)R_y(\pi/2)$ .

**Two-qubit gates:** The only native two-qubit gate in Starmon-5 is the controlled-Z (CZ) gate between any corner transmon  $(Q_0, Q_1, Q_3, Q_4)$  and the central transmon  $Q_2$ . The realization of this gate exploits the flux-controlled



FIG. 4. Schematic diagram of the key instruments in the room-temperature electronics control stack of Starmon-5.

interaction between computational states  $|11\rangle$  and the non-computational state  $|02\rangle$ , where 2 refers to the secondexcited state of the higher-transmon in the pair [9]. We use the Sudden Net-Zero flux pulse [10] to perform the CZ gate. All CZ gates complete within 40 ns.

**Readout:** Native measurement in Starmon-5 is in the computational (Z basis). Measurement is performed with a frequency-multiplexed pulsed measurement of feedline transmission at the frequencies of the readout-Purcell-filter pairs of specified transmons. The response at each frequency is demodulated and integrated (with optimal weight functions [11]) over 0.9  $\mu$ s. The total readout duration, including photon depletion, is 1  $\mu$ s. Starmon supports measurement in the X and Y bases non-natively, realized using pre- and post-rotations.

# V. REPORTED METRICS

**Qubit relaxation and dephasing times:** The relaxation time  $T_1$  and the dephasing time  $T_2^{\text{echo}}$  for each qubit are extracted from standard sliding- $\pi$  pulse and Hahn-echo experiments, respectively [12].

Single-qubit gate fidelity  $F_{1Q}$ : We perform single-qubit Clifford randomized benchmarking (RB) to extract an average error per single-qubit Clifford gate. Taking into account that 1.875 native gates are required on average per Clifford gate, we then extract the average error per native single-qubit gate [13].

**Two-qubit gate fidelity**  $F_{2Q}$ : We perform interleaved RB to extract an average error per two-qubit Clifford gate [14].

**Initialization fidelity**  $F_{\text{INIT}}$ : We obtain a histogram [15] of the analog output of single-shot readout with the qubit initialized (ideally in  $|0\rangle$ ). We perform a double-gaussian fit to this histogram and associate the dominant

(weaker) gaussian to the analog readout for qubit in  $|0\rangle$  ( $|1\rangle$ ). The initialization fidelity is given by the ratio of the area of the dominant gaussian to the total area of the double gaussian.

**Readout fidelity**  $F_{\rm R/O}$ : We perform single-shot readout experiments to determine the probability  $1 - \epsilon_{10}$  of properly declaring measurement outcome 0 when the qubit is prepared in  $|0\rangle$  and the probability  $1 - \epsilon_{01}$  of properly declaring 1 when prepared in  $|1\rangle$ , using the optimal 1-bit discretization threshold. We report the average assignment fidelity [16], given by  $F_{\rm R/O} = 1 - (\epsilon_{10} + \epsilon_{01})/2$ . The reported value corrects for the calibrated initialization error.

#### VI. STRUCTURE OF USER PROGRAMS

To allow for parallel initialization (measurement) in different bases for different qubits, the cQASM parallel construct must be used to group statements. For example, the initialization of qubits  $Q_0$  and  $Q_3$  in the X basis,  $Q_1$  and  $Q_2$  in the Y basis, and  $Q_4$  in the Z basis is specified as follows:

$$\{prep_x q[0,3] \mid prep_y q[1,2] \mid prep_z q[4]\}.$$

Any unspecified qubits will be initialized in the Z basis. The measurement of qubits  $Q_0$  and  $Q_4$  in the X basis,  $Q_1$  and  $Q_3$  in the Y basis, and  $Q_2$  in the Z basis is specified as follows:

{measure\_x  $q[0,4] \mid measure_y q[1,3] \mid measure_z q[2]$ }.

# VII. LIST OF MAJOR CHANGES AND UPGRADES

- April 2020: Added support for generalized initialization and measurement operations.
- May 2020: Shortened the duration of the four CZ gates from 80 to 60 ns.
- May 2020: Added initialization by post-selection to improve initialization fidelities. This post-selection happens behind the scenes and performs sufficient shots to ensure that the user gets back the number of shots they requested.
- May 2020: Increased the maximum possible number of shots per job to 16384.
- June 2020: Improved readout calibration to increase the average  $F_{\rm R/O}$  above 97%.
- June 2020: Added support for arbitrary single-qubit rotations around x and y axes natively, and around the z axis non-natively (see above).
- April 2022: Key upgrade: mid-circuit measurement capability enabled. Up until this point, measurement could only be performed once and at the end of each quantum circuits. This new feature allows multiple measurements to be performed anywhere in the circuit.
- November 2022: Shortened the duration of the four CZ gates from 60 to 40 ns.
- April 2023: Improved readout calibration to increase the average  $F_{\rm R/O}$  above 98%.
- January 2023: Total readout duration reduced from 3 to 1  $\mu$ s.
- January 2023: Added native implementation of  $Z, S, S^{\dagger}, T$ , and  $T^{\dagger}$  using oscillator phase updates (i.e., virtual Z gates).

## VIII. REQUESTS FOR ADDITIONAL MATERIALS

For additional technical information regarding the Starmon-5 processor, cryogenic wiring, control electronics, and reported metrics, please contact G. Ruggero Di Carlo (g.r.dicarlo@tudelft.nl) or Leonardo DiCarlo (l.dicarlo@tudelft.nl).

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