MSc Thesis Project

Characterization of single-photon avalanche diodes and integration with diamond for quantum biosensing

Nitrogen-vacancy (NV) centers in diamond are very promising biosensors. Our goal is to bring the sensing component of such setups down to chip level and realize an on-chip, portable system to perform high-sensitivity and high-accuracy sensing of biosamples, such as detection of magnetic footprint of cancerous cells.

Project Goals:

To achieve this, we will fabricate a diamond substrate with an array of single NV centers and integrate it with a CMOS chip featuring an array of Single-Photon Avalanche Diodes (**SPADs**). These photodetectors will enhance detection sensitivity, speed, and signal-to-noise ratio by efficiently capturing light emitted by individual NV centers in the diamond.

This chip has been fabricated using **40 nm CMOS technology** (TSMC) and includes on-chip quenching circuits.

In this work, you will characterize the fabricated SPADs, implement readout schemes and finally integrate the chip with the diamond, into the desired compact quantum biosensor.

Outcome:

By the end of this MSc thesis project, we anticipate achieving the following outcomes:

- **Characterization** of the fabricated SPADs. This includes both electrical and optical **measurements**, carried out in the EKL lab and our own optical lab.
- **Implementation** of a readout scheme, using FPGA and other tools, which will enable efficient data collection, from the SPADs to the PC.
- Integration of the chip containing SPADs with a diamond substrate. In doing so, you will foster scientific advancement and gain valuable **experience** working in an optical lab whose research focuses on quantum sensing and quantum computing applications.

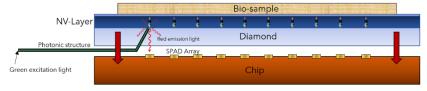


Fig.2 Concept of photonic structure driving the excitation light towards the NV-centers of a diamond integrated in a SPAD array chip.

For more info, contact:

Ryoichi Ishihara <u>r.ishihara@tudelft.nl</u> / Yannis Varveris <u>i.varveris@tudelft.nl</u>



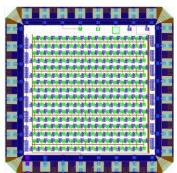


Fig.1 CAD image of the chip containing a 16x16 SPAD array.