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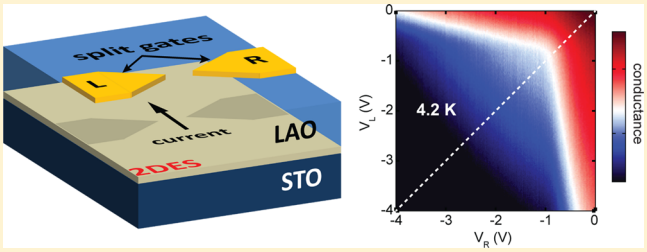
Nanoscale Electrostatic Control of Oxide Interfaces

Srijit Goswami,* Emre Mulazimoglu, Lieven M. K. Vandersypen, and Andrea D. Caviglia*

Kavli Institute of Nanoscience, Delft University of Technology, P.O. Box 5046, 2600 GA Delft, The Netherlands

Supporting Information

ABSTRACT: We develop a robust and versatile platform to define nanostructures at oxide interfaces via patterned top gates. Using $LaAlO_3/SrTiO_3$ as a model system, we demonstrate controllable electrostatic confinement of electrons to nanoscale regions in the conducting interface. The excellent gate response, ultralow leakage currents, and long-term stability of these gates allow us to perform a variety of studies in different device geometries from room temperature down to 50 mK. Using a split-gate device we demonstrate the formation of a narrow conducting channel whose width can be controllably reduced via the application of appropriate gate voltages. We also show that a single narrow gate can be used to induce locally a superconducting to insulating transition. Furthermore, in the superconducting regime we see indications of a gate-voltage controlled Josephson effect.



KEYWORDS: *Oxide interfaces, nanoelectronics, top-gating, split gates, superconducting weak link*

Despite decades of intense study, transition metal oxides continue to reveal fascinating and unexpected physical properties that arise from their highly correlated electrons.[1] Propelled by recent developments in oxides thin film technology it has now become possible to create high quality interfaces between such complex oxides, which reveal a new class of emergent phenomena often nonexistent in the constituent materials.[2,3] In particular, there has been a growing interest in interfaces that host a conducting two-dimensional electron system (2DES).[4,5] This 2DES has been shown to support high mobility electrons,[5−7] magnetism,[8] and superconductivity.[9] In addition to this inherently rich phase space, in situ electrostatic gating can be used not only to alter the carrier density,[10] but it can significantly change the spin−orbit coupling (SOC)[11,12] and even drive transitions from a superconducting to an insulating state.[13]

Bulk transport studies of oxide interfaces have played an important role toward building a better understanding of these new material systems. However, it is becoming increasingly clear that in order to fully grasp the details of the complex coexisting phases at the interface, one must probe the system at much smaller length scales. Recent scanning probe experiments have indeed clearly demonstrated that the electronic properties of the interface can change dramatically over microscopic length scales.[14−16] In this context, nanoscale electronic devices could provide direct information on how such strong local variations in physical properties affect mesoscopic charge transport. Perhaps even more exciting is the possibility of discovering and manipulating new electronic states that are predicted to arise from the interplay between confinement, superconductivity, and SOC.[17] Furthermore, the ability to locally drive phase transitions at the interface could potentially yield technologically relevant oxide-based nanoelectronic devices with novel functionality.[18]

Existing methods for confinement at the interface involve some form of nanoscale patterning, which renders selected portions of the interface insulating, while others remain conducting. These include the use of prepatterned masks,[19] physical etching of the interface,[20] and AFM-based lithography.[21−23] Such techniques have shown promising results and have been used to realize transistor-like nanoscale devices controlled via the field effect from a global back gate or local side gates. However, they do not provide an obvious way to create more intricate device structures that require in situ tunability of the potential landscape. In addition, they suffer from issues such as ion-beam induced damage or long-term stability, which could have a direct impact on device performance.

These hurdles can be overcome by the use of local top gates, which can be conveniently integrated with several oxide interfaces where the top oxide layer itself acts as a high quality gate dielectric. In this device architecture the potential profile in the 2DES can be precisely controlled using appropriate gate voltages, thus making it an extremely flexible and robust platform to build tailor-made nanostructures. Such electrostatic confinement is routinely employed to create low-dimensional systems in traditional semiconductor based 2DESs. It is therefore somewhat surprising that a similar strategy has not been adopted to investigate confinement at oxide interfaces thus far. Large area top-gated devices have indeed been fabricated using a variety of techniques such as sputtering,[24]

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evaporation,[25,26] and in situ deposition.[27,28] However, scaling these structures down has remained a challenge.

Here, we define nanoscale electronic devices in $LaAlO_3$/$SrTiO_3$ (LAO/STO) using patterned top gates that efficiently modify the potential landscape at the metallic interface. We demonstrate that individual narrow gates (down to 200 nm) can completely pinch off the conducting channel and display large on/off ratios with negligible leakage currents. Using two such gates in a split-gate geometry, we can further tune the flow of charge carriers by restricting them to a narrow conducting channel with a width that can be controlled in situ via the gate voltages. At milliKelvin temperatures, when the interface is superconducting, we use a single narrow top gate to drive locally a superconducting to insulating transition at the LAO/STO interface. In the superconducting state, we see evidence for a superconducting weak link with a gate-dependent critical current.

Device fabrication involves pulsed laser deposition for the oxide growth in combination with multiple aligned lithography steps (see Supporting Information for device specific details). Single crystal STO (001) substrates first undergo photolithography or electron beam lithography (EBL), followed by the deposition of 45 nm of amorphous LAO (a-LAO). The a-LAO is deposited at room temperature with an O_2 pressure of 6×10^{-5} mbar and laser fluency of 1 J/cm^2 (repetition rate: 5 Hz). Subsequent lift-off in warm acetone (50 °C) creates an a-LAO mask for the crystalline LAO (c-LAO) deposition. We deposit 12 unit cells of c-LAO at 770 °C with an O_2 pressure of 6×10^{-5} mbar and laser fluency of 1 J/cm^2 (repetition rate: 1 Hz). The film growth is monitored in situ using reflection high-energy electron diffraction (RHEED) confirming layer by layer growth. Finally, a 1 h long postgrowth anneal is performed at 300 mbar O_2 pressure and 600 °C, followed by a cool down to room temperature in the same atmosphere. Under these conditions, the 2DES formed at the LAO/STO interface shows sheet densities of about 3×10^{13} cm^{-2} and field effect mobilities up to 3500 cm^2 V^{-1} s^{-1} at 4.2 K in bulk samples. The patterned top gates are finally defined by an aligned EBL step, followed by electron beam evaporation of 100 nm Au directly on the c-LAO surface.

Figure 1a shows a cross-sectional schematic of a device with a single top gate. An optical image of such a device is shown in Figure 1b, where a narrow (1 μm wide) gate runs across a mesoscopic conducting channel defined at the LAO/STO interface. Figure 1d shows the gate characteristics of this device (Dev1) at 300 K (see Supporting Information for data from similar devices). A constant dc voltage bias of 10 mV is applied across S and D (V_{sd}) and the current (I_{sd}) is measured as a function of the top gate voltage (V_{gate}). The black curve (left axis) shows a typical field effect behavior with complete depletion under the gated region resulting in an on/off ratio of nearly 1000 (shown in the inset). The leakage current (blue trace, right axis) remains below 5 pA in this gate voltage range, thus allowing for reliable measurements of very low currents through the device. The gate width can be reduced even further (in this case to 200 nm), as seen in the (false color) scanning electron microscope (SEM) image of Dev2 (Figure 1c). In Figure 1e we compare the gate response of Dev1 and Dev2 at T = 2 K. Both devices (Dev1-black trace, right axis; Dev2-red trace, left axis) show comparable pinchoff voltages. This is consistent with the fact that they were both fabricated on 12 unit cell LAO deposited under the same growth conditions. We note that each curve consist of 10 consecutive sweeps between

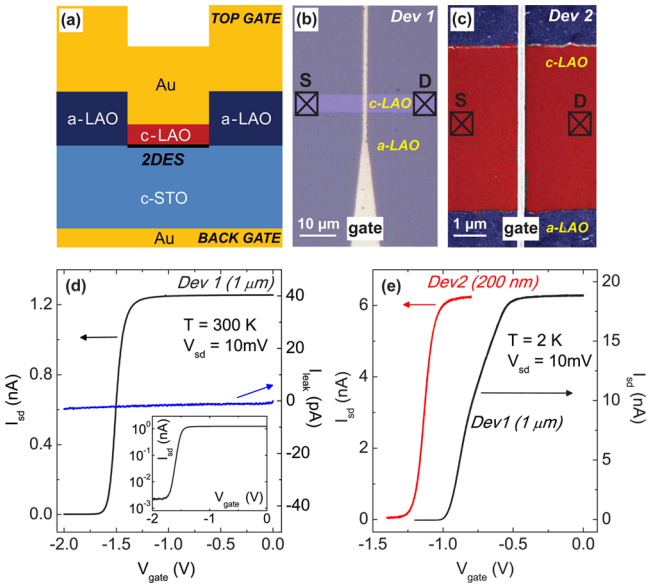

Figure 1. (a) Cross-sectional schematic of a typical top-gated LAO/STO device. The 2DES (indicated in black) is formed at the interface between crystalline LAO (c-LAO) and STO (c-STO). The interface between amorphous LAO (a-LAO) and STO remains insulating. (b) Optical image of Dev1 with a 1 μm wide gate running over the c-LAO. (c) False color scanning electron micrograph of Dev2, which consists of a 200 nm wide top gate. Red/blue areas correspond to conducting/insulating regions. See Supporting Information for full device drawings with the relevant channel dimensions. (d) Gate characteristics for Dev1 at 300 K. Black curve (left axis) shows the variation of source drain current (I_{sd}) with top gate voltage (V_{gate}). Inset: the same curve on a logarithmic scale. Blue curve (right axis) shows the leakage current (I_{leak}) versus V_{gate}. (e) Gate response of Dev1 and Dev2 at 2 K. Each curve consists of 10 consecutive down sweeps from the on to off state.

the on and off states. It is clear that the device completely recovers from the insulating state and is extremely stable over multiple on/off cycles. This is in contrast with recent measurements on bulk top-gated LAO/STO devices where (at low temperatures) going above a critical resistance rendered the interface completely insulating, and conduction could only be revived by thermal cycling.[25] We point out that the two-terminal resistance values are significantly higher than those expected from the bulk mobility and density values mentioned earlier. This discrepancy most likely arises from a contact resistance and/or local regions in the long narrow channel with a significantly higher resistivity.

Having established a reliable gate response from our local top gates, we use two such gates to realize a split gate (SG) geometry, using which charge carriers can be confined to narrow conducting channels. SGs have been successfully used to fabricate quantum point contacts (QPCs) in semiconductor-based 2DESs[29,30] and have provided insights into several aspects of mesoscopic physics (reviewed in ref 31) ranging from the quantum Hall effect to the Aharonov-Bohm effect. They are also extremely sensitive charge detectors[32] and spin filters,[33] and serve as essential components for the creation of lower dimensional systems such as quantum dots.[34] At the LAO/STO interface, such one-dimensional (1D) confinement could possibly give rise to exotic electronic states that emerge from the interplay between 1D superconductivity and SOC.[17] Figure 2a shows an optical micrograph of an SG device on LAO/STO. It consists of a left (L) and right (R) gate, both of

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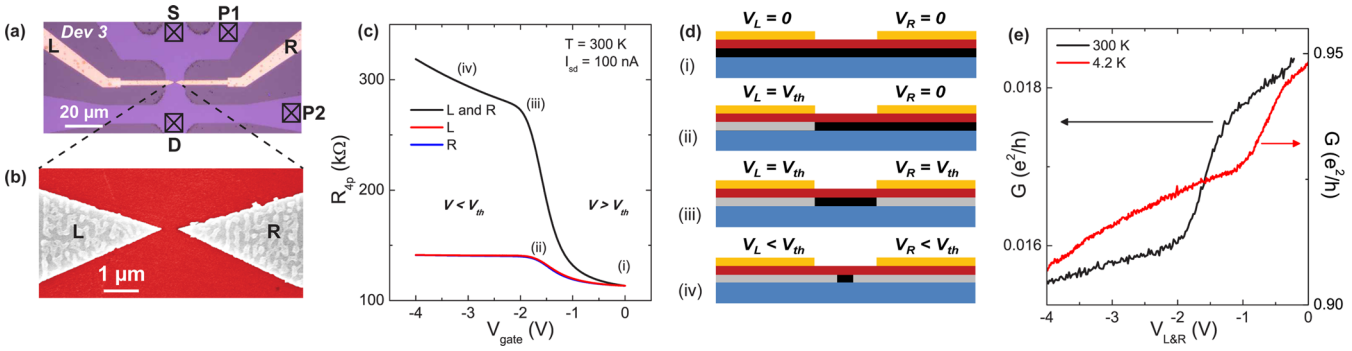

Figure 2. (a) Optical and (b) SEM images of a split gate (SG) device which comprises of a left (L) and right (R) gate. (c) Four-probe resistance (R_{4p}) measurements (at 300 K) comparing the gate action of the individual gates (red and blue curves) with that of both gates together (black curve). Note that the red and blue curves show an excellent overlap, which makes it hard to distinguish between the two in the plot. The labels [(i)−(iv)] mark different transport regimes in the operation of the SG device. The corresponding density variations at the LAO/STO interface are shown schematically in (d), where black/gray represent conducting/insulating regions in the 2DES. (e) Two-probe voltage biased measurements: Conductance, G versus $V_{L\&R}$ at 300 K (black curve) and 4.2 K (red curve). See Supporting Information for device drawings with the relevant channel dimensions.

which start off 2.5 μm wide and taper down to a narrow point. Figure 2b shows an SEM image of the active device region. We have studied devices with tip separations of approximately 400 nm (Dev3) and 250 nm (Dev4), and both show qualitatively similar features. Here we focus on Dev3 (results from Dev4 can be found in the Supporting Information).

We begin by studying the room temperature four probe resistance (R_{4p}) across the SG, as a function of the individual (L, R) gates. A 100 nA dc current is applied between S and D (I_{sd}), and resistance is measured between contacts P1 and P2 (see Figure 2a). For these measurements no back gate voltage was applied. When the SG is held at zero ($V_L = V_R = 0$), the carrier density in the entire channel is uniform. This is shown schematically in Figure 2d (top panel), where the uniform black area represents a wide channel with no density variations. The corresponding point in the R_{4p} versus V_{gate} plot (Figure 2c) is marked by the label (i). As one of the gates (say L) is made more negative, the carriers below this gate are depleted, resulting in a sharp increase in R_{4p} (red curve). However, at a critical threshold voltage (V_{th}) the region below R is completely depleted, indicated by (ii) in Figure 2c,d (gray areas represent depleted regions in the 2DES). Throughout, we define V_{th} as the gate voltage where the magnitude of this slope is maximum. Beyond V_{th} the gate action is weaker, because depletion must now occur sideways, thereby resulting in a lower slope in the R_{4p} versus V_{gate} curve. Sweeping only L (instead of R) should be electrostatically equivalent to the situation described above. This is reflected directly in transport by the excellent overlap between the red and blue curves. If both R, L are swept together the response is much stronger (black curve). When $V_L = V_R = V_{th}$ [label (iii)] a narrow constriction is formed in the 2DES, whose width is determined by the geometry of the split gates and the electrostatics of the system. Finally, going to even more negative voltages with L and R together [label (iv)] squeezes this channel further. Thus, through an appropriate device design and suitable gate voltages, it is clearly possible to electrostatically define nanoscale constrictions at an oxide interface, even at room temperature.

Next, we study this SG device (Dev3) at cryogenic temperatures in a two probe configuration. Figure 2e shows the variation of the conductance (G) with $V_{L\&R}$ (i.e., both L and R swept together) at 300 K (black curve, left axis) and 4.2 K (red curve, right axis). Two things are immediately apparent from these plots. First, the conductivity of the system increases significantly as the temperature is lowered, which is expected for such metallic samples. Second, V_{th} shifts to less negative voltages upon cooling down. It has been suggested that the sheet density can reduce with temperature as a result of carrier freeze-out.[7] Such a reduction in the sheet density with temperature could qualitatively explain the observed shift in V_{th}, as it now becomes much easier for the SG to deplete the carriers. However, at these temperatures an even more striking effect appears in the gate response of the SGs, which only becomes apparent through detailed phase space maps of the conductance versus the individual gates.

Figure 3a,b shows two such maps of G at 300 K and 4.2 K, respectively. It is worth pointing out that these maps are typically acquired over several hours, during which the device does not show any switches or obvious drifts, confirming the stability and robustness of these gates. Furthermore, both gates (L and R) have a nearly identical influence on the 2DES at the interface. This is evident from the high degree of symmetry across the diagonal (white dashed line). Such a symmetric response of the two gates can be expected if the 2DES has a homogeneous density. However, inhomogeneities in the gated regions could give rise to a reduction in this symmetry (as seen for Dev4 in the Supporting Information). The entire phase space can be divided into two distinct regions. The blue portion (lower G) corresponds to a situation when both L and R have been driven beyond their respective threshold voltages. The red area (higher G), thus reflects the complementary scenario, where either one (or none) of the gates have crossed V_{th} (black circles indicate the position of V_{th} for each of the gates with the other held at zero). The narrow white band therefore separates these two electrostatically distinct regimes and provides information about the effective region of influence of the individual gates and the extent of cross-talk between them. These effects can be examined in a more consistent manner by taking a derivative along one of the gate axes.

Figure 3c,d shows the corresponding numerical derivatives taken along the V_R axis (dG/dV_R). As mentioned earlier, the maximum in dG/dV_R occurs at V_{th} associated with gate R. At 300 K, as V_L is made more negative the position of the threshold does not change, indicating that there is practically no cross-talk between the gates. This is perhaps not so surprising considering the fact that the gates are very close (~5 nm) to

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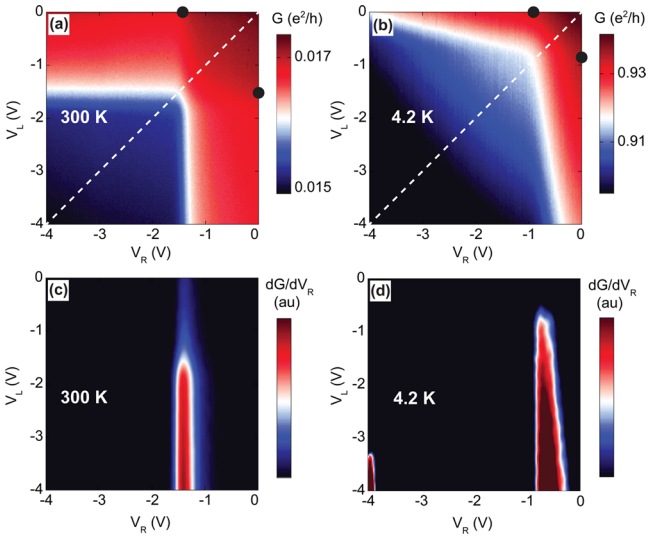

Figure 3. 2D maps of conductance (G) as a function of left/right (L/R) split gate voltages (V_L/V_R) at (a) T = 300 K and (b) T = 4.2 K. The gate voltage step (for both V_L and V_R) is 20 mV. Black circles mark the positions of the threshold voltage for either gate with the other held at zero. Symmetry about the white dashed line indicates comparable gate action from both L and R. (c,d) Plots of the corresponding numerical derivatives taken along the V_R axis (dG/dV_R). The maximum in dG/dV_R indicates the threshold voltage for gate R. It is independent of V_L at 300 K but shows a distinct shift at 4.2 K, indicating cross-talk between L and R at low temperatures.

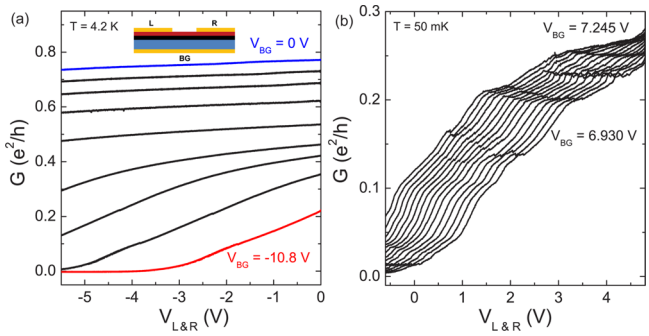

Figure 4. (a) The conductance (G) of the nanoconstriction formed by the split gates can also be tuned using the back gate (BG). While G does not change appreciably with $V_{L\&R}$ when V_{BG} = 0 V (blue curve, a similar trace is also shown in Figure 2e) for V_{BG} = −10.8 V it is possible to completely deplete the channel using split gates (red curve). Intermediate (black) curves correspond to V_{BG} = −1.8, −3.6, −5.85, −8.1, −9.45, −9.9, and −10.35 V. (b) Modulation of G with $V_{L\&R}$ at milliKelvin temperatures due to mesoscopic effects in the conducting channel. The modulations evolve continuously as a function of BG.

the interface, and therefore most of the electric field lines go directly downward, creating a sharp potential profile with minimal spreading of the electric field. However, at 4.2 K the situation is rather different. V_L obviously has a distinct effect on the threshold voltage for R, shifting it to less negative voltages, as V_L becomes more negative. This suggests that V_L has a significant influence on the region below R, which is in contrast with the observations at 300 K. Such a modification of the electrostatics could possibly be related to the fact that STO is an incipient ferroelectric, thereby exhibiting a strong increase in its permittivity at low temperatures.[35] A combination of this large permittivity (~10^4 at T = 4 K) along with imperfect screening from the 2DES could provide a viable mechanism for the observed cross-talk between the gates. As the carrier density below L is reduced, the extent of screening from the 2DES below L reduces. This in turn allows electric field lines to go through the STO, resulting in a significant field effect in the region below R. Though a likely explanation, the feasibility of such a scenario ultimately needs to be tested using electrostatic simulations with appropriate parameters for the screening lengths at the LAO/STO interface.

In addition to local top gates, the global back gate can also modify the electrostatics at the interface, thus providing additional control over transport through electrostatically defined nanostructures. Though our SG devices show clear evidence of confinement, the relatively large separation between the gates (as compared to the distance of the gates from the 2DES) makes it difficult to pinch off the channel using just the top gates. However, by reducing the sheet carrier density via moderate negative voltages on the back gate (BG), we could indeed deplete the constriction completely, as seen in Figure 4a. In this geometry the entire 0.5 mm thick STO substrate is used as the back gate dielectric. At V_{BG} = 0 V, the channel remains fairly open in this top gate voltage range (blue trace) but shows a clear pinch-off for V_{BG} = −10.8 V (red trace). We note that in all the devices studied here, we observed a strong hysteresis in the BG action at low temperatures. As the BG is taken to positive values, G typically saturates for V_{BG} > 20 V. Subsequently, going back to V_{BG} = 0 V renders the sample highly insulating. However, the conductance can be completely recovered by taking the top gate to positive voltages, which suggests that the effect arises primarily from the region below the local gates. Such an effect was not observed in larger Hall bars (channel width ~500 μm), fabricated in a similar fashion but without top gates.

Figure 4b shows the variation of G with $V_{L\&R}$ at T = 50 mK for a small range of BG voltages. This data was obtained after the BG was first swept up to 22.5 V and then reduced to 7.245 V. As described above, at $V_{L\&R}$ = 0 V the sample is now less conductive, but sweeping $V_{L\&R}$ to positive values increases I_{sd}. It is also evident that there is a finer structure that emerges at these low temperatures, which is clearly absent at T = 4.2 K (Figure 4a). These modulations in conductance are highly reproducible and show a continuous evolution with V_{BG}. We attribute this structure to mesoscopic effects that arise from disorder in the conducting channel. We believe that the integration of such split-gate devices with higher mobility oxide interfaces with significantly longer mean free paths[5,7] should enable studies of mesoscopic transport in the 1D limit.

Thus far we have concentrated on the flow of normal electrons through devices defined via local top gates. Of course, one of the remarkable properties of the LAO/STO interface is that it can also host 2D-superconductivity.[9] Furthermore, bulk studies have shown that reducing the carrier density at the interface with a global back gate results in a quantum phase transition between superconducting and insulating ground states.[13] The ability to locally alter the ground state of the interface at the nanoscale provides the opportunity to create gate-tunable superconducting circuit elements (e.g., Josephson junctions), which may enhance our understanding of the microscopic nature of superconductivity at the interface. To study the effects of a local top gate on the superconductivity we cooled down Dev2 (see Figure 1c for SEM image) to T = 50 mK and recorded current−voltage (I−V) characteristics as a function of V_{gate} in a four probe configuration (with BG fixed at

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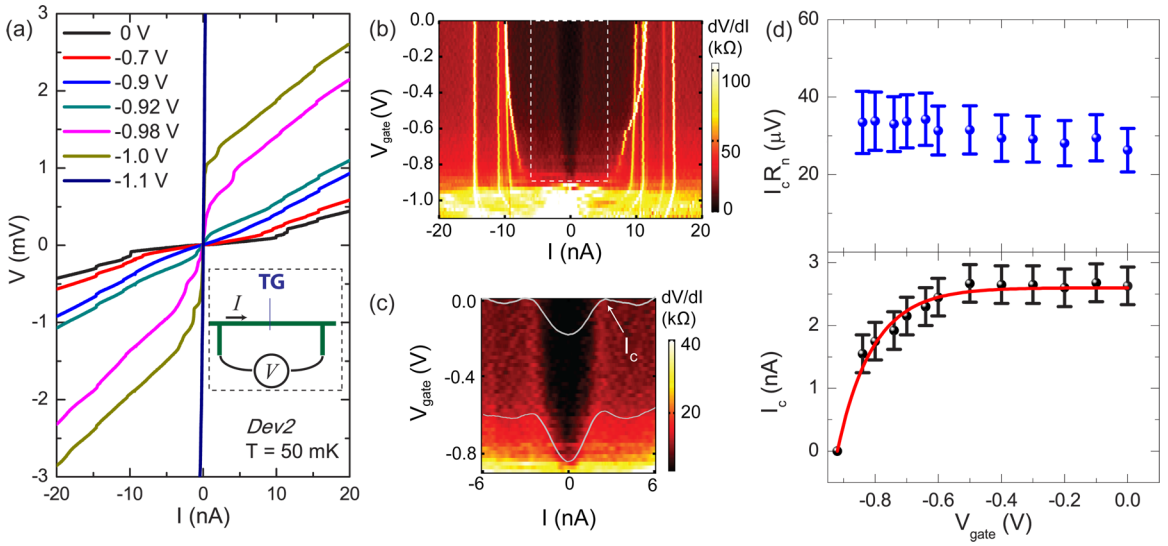

Figure 5. (a) A local superconducting to insulating transition induced by the top gate. Inset: schematic (to-scale) of the device and measurement configuration. (b) A 2D map of differential resistance (dV/dI) as a function of I and V_{gate}. (c) A closer view of the region enclosed by the dashed lines in (b), with line traces at $V_{gate} = 0$ V and $V_{gate} = -0.6$ V (d) Lower and upper panels show the critical current (I_c) and I_cR_n product respectively of a gate-tunable weak link. Red line is a guide to the eye.

zero). In Figure 5a we plot a few representative $I-V$ traces at different values of V_{gate} (inset shows a to-scale schematic of the measurement configuration). These curves show a clear transition from a superconducting state ($V_{gate} = 0$ V, black trace) to an insulating state as V_{gate} is made more negative. This insulating state is evident from a gaplike structure that emerges for $V_{gate} < -0.9$ V and grows in size as the gate voltage is further reduced. Though previous studies with large top gates have shown some gate dependent modulation of the critical current,[25] we believe that a local superconducting-insulating transition has thus far not been observed at the LAO/STO interface.

Figure 5b shows a 2D plot of differential resistance dV/dI (obtained via numerical differentiation of the gate-dependent $I-V$ traces) as a function of V_{gate} and I. Two important features to note in this plot are (i) strong peaks that occur at relatively high currents (10−15 nA) and (ii) a weaker peak at much lower currents (<3 nA), which closes as V_{gate} is made more negative and finally disappears around the superconducting−insulating transition. The stronger set of peaks reflect the current driven superconducting to normal transition in the areas outside the top gated region (we comment further on them toward the end). To understand the origin of the strongly gate-dependent structure at lower currents, we explore the possibility that the region under the top gate acts as a weak link between the superconducting reservoirs on either side. Figure 5c shows the dV/dI map in a smaller range (indicated by dashed rectangle in Figure 5b) with two representative line traces at $V_{gate} = 0$ V and $V_{gate} = -0.6$ V. We start by associating a critical current (I_c) with the first local maximum in dV/dI. Figure 5d (lower panel) shows that I_c is roughly constant from $V_{gate} = 0$ V to $V_{gate} = -0.5$ V, below which it begins to drop more rapidly and finally disappears at $V_{gate} = -0.92$ V (red line is a guide to the eye). In the upper panel, we plot the product of I_c and R_n (where R_n is the resistance just above I_c), which remains roughly constant over the entire gate voltage range, a characteristic signature of a Josephson junction. For $T \ll T_c$ (T_c is the critical temperature of the superconducting reservoirs), we expect $eI_cR_n \approx \alpha\Delta$, where Δ is the superconducting gap in the reservoirs, e is the electronic charge, and α depends on the microscopic details of the weak link and can take values from ∼1.5−3.[36] The weak link can in general be a tunnel barrier, a superconductor, or a normal metal. Interestingly, for the LAO/STO system all three scenarios are possible, and the current experiments cannot precisely determine the actual microscopic nature of the weak link. However, using the fact that we experimentally determine eI_cR_n ∼ 30 μeV, we estimate that Δ ∼ 10−20 μeV. Though these values are slightly smaller (roughly by a factor of 3) than recent measurements of Δ via tunneling spectroscopy,[28] they are consistent with the lower T_c ∼ 100 mK of our samples (see Supporting Information). We note that similar observations of a gate-tunable weak link at the surface of STO have also recently been reported.[37]

Finally, we remark on the evolution of the peaks in dV/dI at higher values of I and associated with superconducting-normal switching of the area outside the top gated region. We associate the multiple switches with inhomogeneities in the long (150 μm) and narrow (5 μm) conducting channel across which the measurements were performed. Most of the peaks run parallel to each other, showing hardly any gate-dependent shifts until about $V_{gate} = -0.9$ V, which is close to where the superconducting-insulating transition occurs. Interestingly, below $V_{gate} = -0.9$ V these peaks start coming together more rapidly. Though we do not have a complete understanding of this behavior at the moment, we present two possible explanations. The first possibility is that the significantly higher resistance of the insulating state gives rise to Joule heating that increases the local electronic temperature, thereby reducing the critical current of the neighboring regions. The second possibility relates to the earlier discussion (in the context of split gates), whereby electric field lines from the top gate could potentially spread out significantly once the density below the gate is reduced. In this scenario, the evolution of the peaks could be explained by the fact that the electrostatic region of influence of the top gate extends significantly beyond its geometric dimensions, thereby reducing the critical current in the neighboring regions. In contrast to our current device

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geometry, we believe that devices with significantly wider superconducting banks would be more suitable for the study of the Josephson effect. In such devices, the ungated regions would have a much larger critical current than the weak link, and the strong influence of local inhomogeneities could possibly be suppressed, thereby allowing for a clearer interpretation of the results.

In conclusion, we have demonstrated that top gating can be used to create electrostatically confined nanostructures at the LAO/STO interface. These gates show excellent performance and stability from room temperature down to 50 mK. Not only do they allow us to control the electrostatic landscape through which normal electrons flow, they provide a promising route to locally control the electronic ground state of the interface. The inherent flexibility in the design of such top-gated structures opens up a new and versatile platform for creating a variety of gate-tunable nanostructures at oxide interfaces.

■ ASSOCIATED CONTENT

Supporting Information

A detailed description of the fabrication process and additional data from other top-gated devices. This material is available free of charge via the Internet at http://pubs.acs.org.

■ AUTHOR INFORMATION

Corresponding Authors

*E-mail: s.goswami@tudelft.nl (S.G.).
*E-mail: a.caviglia@tudelft.nl (A.D.C.).

Notes

The authors declare no competing financial interest.

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