Wafer-scale silicon for quantum computing

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Enrichment of the spin-zero ^{28}Si isotope drastically reduces spin-bath decoherence in silicon[1, 2] and has enabled solid state spin qubits with extremely long coherence[3, 4] and high control fidelity[5–7]. The limited availability of isotopically enriched ^{28}Si in industrially adopted forms [8], however, is a major bottleneck to leverage CMOS technology for manufacturing qubits with the quality and in the large numbers required for fault tolerant quantum computation[9, 10]. Here we show wafer-scale epitaxial growth of isotopically enriched ^{28}Si/^{28}SiO$_2$ stacks in an industrial CMOS fab, and demonstrate highly uniform films with an isotopic purity greater than 99.92%. We induce a two dimensional electron gas, the cornerstone of silicon spin qubit architectures, at the isotopically enriched semiconductor/oxide interface by electrical gating. To confirm the high quality growth, we perform electrical probing and show matching properties for fin transistors in ^{28}Si and natural Si, fabricated using the same high volume manufacturing process. Quantum transport measurements at cryogenic temperature validate wafer-scale ^{28}Si as a suitable material to host qubits. The establishment of an industrial supply of isotopically enriched Si, previously thought to be a major hurdle, provides the foundation for high volume manufacturing of long-lived spin qubits.

Isotopically enriched silane ($^{28}SiH_4$) as a gas precursor for ^{28}Si chemical vapour deposition has been employed to deposit ^{28}Si epilayers used in the early single-qubit experiments[3–5, 8]. More recently $^{28}SiH_4$ was used in a pre-industrial CMOS facility to grow high quality ^{28}Si epi-wafers[11]. Here, we show the crucial step of fully integrating ^{28}Si into a manufacturing CMOS fab, validated by quantum transport measurements. The schematics shown in Fig. 1 illustrate the supply chain for isotopically enriched precursors for wafer-scale epitaxial growth of ^{28}Si.. A silicon-tetrafluoride gas (SiF_4) with natural abundance of ^{28}Si of 92.23% is isotopically enriched in ^{28}Si to greater than 99.92% by centrifuge separation. The $^{28}SiF_4$, with a residual ^{29}Si concentration of lower than 800 ppm, is then reduced to obtain $^{28}SiH_4$. $^{28}SiH_4$ gas cylinders have been installed for use in a state-of-the art chemical vapor deposition tool of a 300 mm fabrication line to deposit ^{28}Si epilayers. It is crucial that the chemical purity of gas precursors is maintained throughout the supply chain. The growth process starts with the deposition of 1 μm of intrinsic natural Si on a high-resistivity 300 mm Si(100) wafer followed by a 100-nm-thick intrinsic ^{28}Si epilayer. The epilayer is then thermally processed for the formation of a high quality 10-nm-thick $^{28}SiO_2$ layer.

In Fig. 1 we compare the morphology and composition of the grown stack at the center and the edge of the 300 mm wafer. No difference in surface or interface roughness, composition, and purity could be observed across the wafers, indicating a uniform film deposition. Atomic force microscopy shows a uniform and almost defect-free surface with a root mean square surface roughness of 0.2 nm. Secondary ion mass spectroscopy of isotopes ^{28}Si, ^{29}Si, and ^{30}Si demonstrates a high purity film with a residual concentration of non-zero-spin nuclei ^{29}Si reduced from 4.76% in the Si buffer to less than 0.09% in the purified epilayer. The concentration of common background contaminants C and O is below the detection limit of 4×10^{17} cm^{-3} and 1×10^{18} cm^{-3}, respectively. High resolution transmission electron microscopy shows the ^{28}Si/$^{28}SiO_2$ interface is flat down to 1-2 atomic layers over ranges that are for practical reasons meaningful for Si quantum dot spin qubits. No dislocations or stacking faults are visible in the epilayer. The sharpness of the interface, the negligible density of defects in the lattice, and the associated electron diffraction pattern highlight the film quality and good control over the growth process.

Isotopically enriched ^{28}Si transistor test structures (15 nm fin width and 50 nm gate length) were fabricated in the 300 mm high volume manufacturing line. We used a standard fab process flow comprised of the following steps: fin patterning, shallow trench isolation, high-κ metal gate-stack, and contacts. Figure 2 shows the electrical characterisation of these transistors by whole wafer electrical probing at room temperature. Current-gate voltage measurements (Fig. 2(a)) from devices on ^{28}Si (red curve) and natural Si (blue curve) substrates

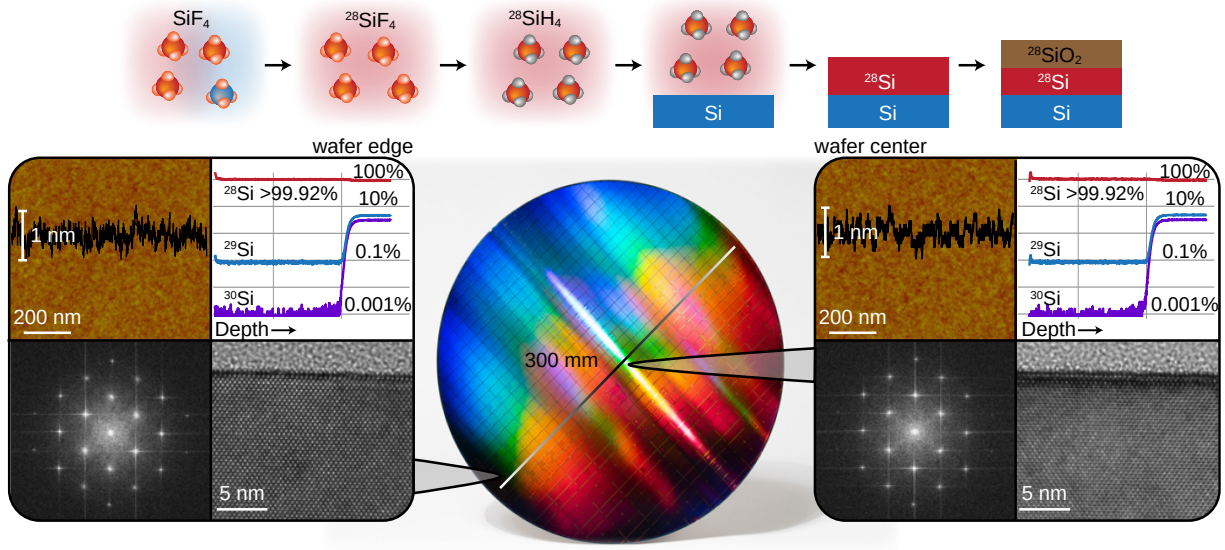

Figure 1. Central panel: a 300 mm Si(100) wafer with epitaxial ^{28}Si and transistor test structures, processed in a CMOS high volume manufacturing fab. Top panel: supply chain for $^{28}SiH_4$ gas precursor. Side panels show the material characterisation at the center and at the edge of the as-grown wafer (right and left panels, respectively). The characterisation includes (from top left, clockwise): atomic force microscopy of the smooth surface with line scan; compositional analysis (depth range of 160 nm) by secondary ion mass spectroscopy of isotopes ^{28}Si (red), ^{29}Si (blue), ^{30}Si (purple); high-resolution transmission electron microscope image of the $^{28}Si/^{28}SiO_2$ interface; electron diffraction patterns with sharp and equally spaced peaks.

are overlaid and show healthy and matching device characteristics. We observe a similar cross-wafer variation of key transistor metrics (Fig. 2(b)-(e)), indicating that ^{28}Si and natural Si processes behave similarely through all of the key processing steps required for qubit fabrication. These results demonstrate the successful integration of ^{28}Si in a 300 mm CMOS manufacturing line; a first step toward the large-scale integration of ^{28}Si qubits.

To evaluate relevant material properties for semiconductor qubits such as carrier mobility, critical density, and valley splitting energy, we use quantum transport measurements in micron-scale Hall-bar devices at low temperature. Large mobility and small critical density associated with the metal-insulator transition indicate material uniformity and low disorder at the critical confining interfaces. These properties are beneficial for obtaining reproducible quantum dots at intended locations on the substrate. Valley splitting quantifies the energetic separation between the ground state used for computation and the lowest excited state, and a large splitting energy is beneficial for qubit operation[12].

Figure 3(a) shows the optical micrograph and the key elements of a Hall-bar shaped transistor. The devices were fabricated in an academic cleanroom environment, starting from coupon-sized samples diced from the original $^{28}Si/^{28}SiO_2$ 300 mm wafer and using electron beam lithography and lift-off additive techniques. The Hall-bar transistor has an equivalent SiO_2 oxide thickness (EOT) of 17 nm due to an additional 17-nm-thick Al_2O_3 layer deposited on top of $^{28}SiO_2$ to emulate the additional steps used in multi-layer gate-defined qubits.

The electrical characterisation of the device was performed at a temperature of 1.7 K using standard low frequency lock-in techniques to measure the longitudinal (ρ_{xx}) and transverse (R_{xy}) resistivity, electron mobility μ, and Hall carrier density n as a function of gate voltage V_g and external perpendicular magnetic field B (See Methods).

A DC voltage applied to the top gate (V_g) accumulates a two-dimensional electron gas (2DEG) at the $^{28}Si/^{28}SiO_2$ interface which conducts above a turn-on voltage of $V_{to} = 1.36$ V. For values below V_{to} no current flow is observed in the device up to a temperature of $T = 23$ K, confirming the insulating behavior of the intrinsic ^{28}Si film at low temperature. For $V_g > V_{to}$ (Fig. 3(b)) we measure a linear increase in the Hall density n as a function of V_g. The experimental capacitance $C = e\, dn/dV_g$ matches within 5% the expected value for the given EOT.

Figure 3(c) shows the density-dependent mobility. Above a critical density n_c, required to establish metallic conduction in the 2DEG, the mobility rises sharply due to screening from charged impurity Coulomb scattering. A maximum mobility of 9800 cm^2/Vs is reached at a characteristic density $n_m = 1.13 \times 10^{12}$ cm^{-2}. Beyond n_m the mobility drops due to surface-roughness scattering at the $^{28}Si/^{28}SiO_2$ interface [13–15]. We estimate a $n_c = 2.16 \times 10^{11}$ cm^{-2} at 1.7 K by extrapolating the mobility μ vs. $\log(n)$ above the critical density[16] to zero, shown in Fig. 3(d). Both the mo-

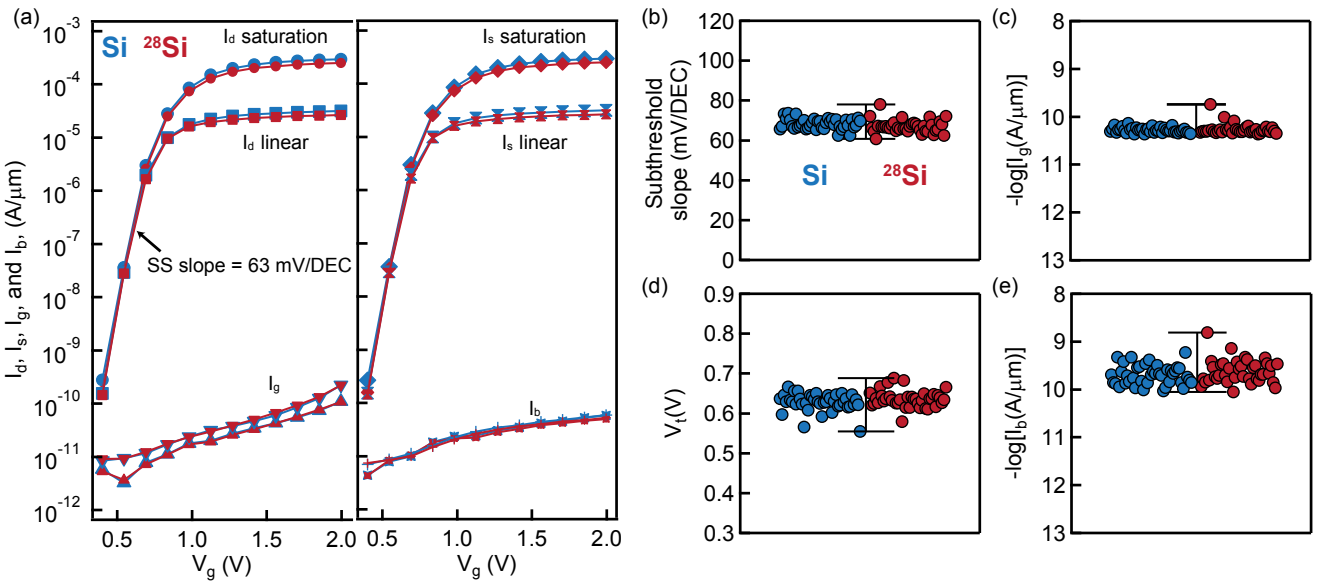

Figure 2. Performance benchmarking between ^{28}Si (red) and Si (blue) transistors fabricated with large-scale industrial manufacturing processes and measured by on-wafer room-temperature probing. (a) Drain current I_d, source current I_s, gate current I_g and body current I_b as a function of gate voltage V_g for a single ^{28}Si and Si transistor. Measurements were performed at source-drain bias of $V_{sd} = 0.05$ V (linear regime) and $V_{sd} = 0.5$ V (saturation regime). Identical measurements were carried out across the wafer for comparison of (b) subthreshold slope, (c) gate leakage, (d) threshold voltage V_t, and (e) body leakage.

bility and critical density obtained in the isotopically enriched ^{28}Si/^{28}SiO$_2$ stack are qualitatively comparable to the values $\mu \approx 1 - 2 \times 10^4$ cm^2/Vs and $n_c \approx 10^{11}$ cm^{-2} previously reported for high-mobility MOSFETs in natural Si at low temperatures[17–19]. Therefore, these results support the use of industrial ^{28}Si/^{28}SiO$_2$ stacks for spin qubits fabrication.

Transport characterisation at high magnetic field allows measurements of the effective mass m^* and quantum lifetime τ_q, from which we deduce upper bounds for the valley splitting energy and estimate the g-factor. Figure 3(e) shows the longitudinal magnetoresistivity with Shubnikov-de Haas (SdH) oscillations minima aligned to quantum Hall plateaus in R_{xy}. SdH oscillations start at B_{eff}= 1 T and spin degeneracy is resolved at the even filling factor $\nu = 10$. We do not observe odd filling factors, indicating that valley degeneracy is not resolved under these measurement conditions. An electron effective mass $m^* = 0.19m_e$ and a quantum lifetime $\tau_q = 0.69$ ps are extracted by fitting, respectively, the damping of SdH oscilation amplitude with increasing temperature (Fig. 3(f)) and their envelope[20–23] (See Supplemental Information). The effective mass value is in agreement with measurements performed on natural Si[24].

The obtained τ_q implies a Landau Level broadening $\Gamma \approx \hbar/2\tau_q = 477$ μeV, which sets an upper bound to valley splitting at the investigated density and magnetic field. For comparison, a valley splitting energy of 275 μeV was measured in ^{28}Si quantum dots fabricated on identical wafers in an academic environment[25]. The onset of spin-splitting at $B_S = 4.3$ T implies that the Zeeman energy $g\mu_B B_S \simeq \Gamma$, where μ_B is the Bohr magneton. From this a g-factor of $g = 1.92 \pm 0.07$ is estimated, which is close to the expected single-particle value of $g = 2$.

In conclusion, we demonstrate the integration of isotopically enriched ^{28}Si on 300 mm wafers in a high volume manufacturing CMOS environment. We study the transport characteristics of two types of devices: i) nanoscale transistors based on Si fins, entirely fabricated in a 300 mm line using standard transistor process modules; and ii) micron-scale Hall-bar transistors fabricated in an academic environment. The electrical characteristics of transistor devices on isotopically enriched ^{28}Si validate utilization of these stacks in front-end fab processing. Quantum transport characterisation of the Hall-bar transistors at cryogenic temperatures show the 2DEG at the ^{28}Si/^{28}SiO$_2$ interface to have excellent properties for hosting spin qubits. Mobility and critical density for these stacks are among the best reported for equivalent oxide thicknesses, with the potential to achieve large valley splitting.

The advanced process control attainable by performing the entire device fabrication process in the high volume manufacturing environment is expected to further decrease disorder at the critical silicon/oxide interface, thereby increasing μ and decreasing n_c. Overall, these results serve as a first step toward the fabrication of ^{28}Si quantum dot spin qubits in a state-of-the-art semiconductor manufacturing line. This opens an important avenue to advance spin qubit performance because many of

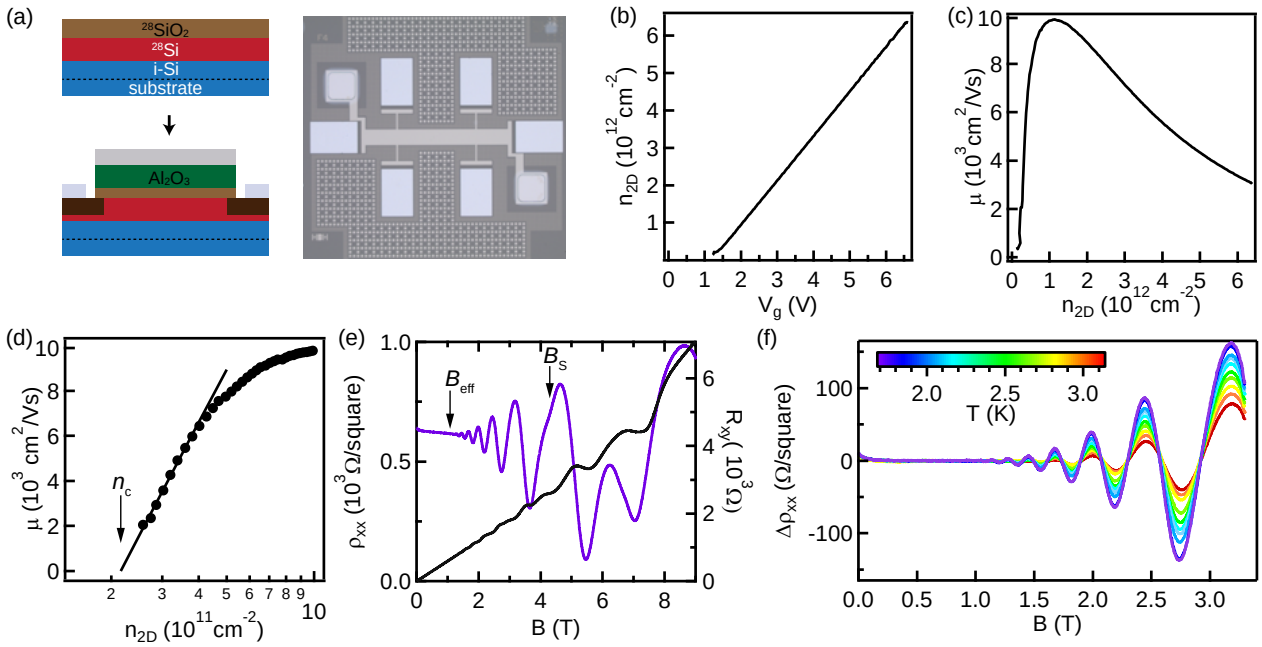

Figure 3. (a) Hall-bar device fabrication schematics starting from the 300 mm $^{28}SiO_2/^{28}Si/Si(100)$ stack, followed by coupon-size processing to obtain n^{++} implants (brown), an additional Al_2O_3 dielectric layer (green), metallic ohmic contacts and top gate (gray). The optical micrograph of the final device shows the multi-terminal geometry used for Hall measurements. (b) Linear relationship between 2DEG Hall density n and top gate voltage V_g at $T = 1.7$ K. (c) Channel mobility μ as function of n. (d) Mobility-density curve in the lowest density range. Solid line is the linear fit used to extrapolate the critical density. (e) Magnetotransport at $n = 1.11 \times 10^{12}$ cm^{-2} and $T = 1.7$ K. The arrows indicate the magnetic field at which SdH oscillations and Zeeman spin-splitting are resolved. (f) Temperature dependence of the SdH oscillation amplitude in the range $T = 1.7$-3.1 K, after polynomial background subtraction.

the limiting challenges, such as non-uniformities in the gate patterns and quality of the dielectric interfaces, are fundamentally related to process control.

METHODS

Hall bar transistors fabrication and electrical characterisation. Starting from coupon-sized samples diced from the original $^{28}Si/^{28}SiO_2$ 300 mm wafer, highly doped n^{++} regions are obtained by P-ion implantation followed by activation annealing in N_2 environment. Multiple ohmic contacts are deposited by e-beam evaporation of Al. The top gate defining the transistor channel is fabricated by depositing a layer of Ti/Pd on top of 17 nm of Al_2O_3 grown by atomic layer deposition at 300°C. The final device is annealed in forming gas at 400°C to reduce the structural damage induced by e-beam lithography[19, 26]. The electrical characterisation of the device was performed at a temperature of 1.7 K using standard four-terminal low frequency lock-in techniques with a constant source-drain excitation voltage of 1 mV. Longitudinal (ρ_{xx}) and transverse (R_{xy}) resistivity were measured as a function of carrier density, controlled by V_g, and external perpendicular magnetic field B. The Hall carrier density n and electron mobility μ are calculated using the relationships $R_{xy} = (ne)^{-1}B$ and $\mu = (ne\rho_0)^{-1}$, respectively, where e is the elementary charge and $\rho_0 = \rho_{xx}(B{=}0\text{T})$.

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ADDITIONAL INFORMATION

Supplemental information accompanies this paper.

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