Supplementary Part: Towards high mobility InSb nanowire devices

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S1. Optimized fabrication recipe

- Substrate cleaning: 10 minutes remote oxygen plasma cleaning (Tepla 300 Plasma Asher) of the p^{++}-Si substrate covered with 285 nm dry thermal SiO_2 with pre-defined Au alignment markers (oxygen pressure 1 mbar, plasma power 600 W). All substrates were from the same wafer.
- Wire deposition: deterministic positioning of wires using a setup similar to that described in ref. [35]. Wires were always taken from the same section on the same growth chip.
- SEM imaging of the nanowires with surrounding alignment markers. Images are used for the subsequent design of the contacts.
- Spin resist: PMMA 950A4 at 4 krpm, baking $>$ 15 minutes at a temperature of 175 °C.
- Electron beam writing of the contact design.
- Development: MIBK:IPA 1:3 60 s, IPA 60 s.
- Ar etching (AJA International sputtering system) using rf-plasma: pressure 3 mTorr, Ar flow 50 sccm, power 100 W, duration 300 s, no rotation of the sample holder. A voltage of 300 V is applied to the sample holder.
- Contact deposition: e-beam evaporation of Ti/Au 5/145 nm with deposition rate 0.5 Å/s and 2 Å/s respectively.
- Lift-off in acetone: the sample with acetone is heated for several hours and left in acetone for $\geq$ 12 h.
- Samples were stored in an Ar glove box between fabrication and mounting.

S2. Measurements

- Sample space (IVC) evacuated for $\sim$ 60 hours after mounting (insert type: Desert Cryogenics).
- For thermalisation, He of $\sim$10 mbar is added to sample space at room temperature before cooling down the devices. During low-temperature measurements samples are kept in a vacuum environment.
- $G(V_g)$ measured using 10 mV bias, gate voltage range from -6 V to $+30$ V with sweep rate 6 mV/50 ms. Measured in forward and reverse sweep direction.
- To check a possible sweep rate dependence of $G(V_g)$, gate voltage steps of 0.15, 0.3, 0.6, 1.5, 3, 6, 15, 30 [mV/(50 ms)] is used both in forward and reverse sweep direction. No dependence on sweep rate was found.

S3. Device capacitance

The capacitance for different channel lengths is calculated with a 3D Laplace solver for a realistic device geometry including the metallic leads. Here the wire is assumed to be metallic. Then, for a more accurate representation of the device capacitance and to account for quantum confinement effects, 2D Schrödinger-Poisson solver was used and its result is compared with the capacitance calculated with 2D Laplace solver. A reduction of capacitance by 20% is found for the case of quantum mechanical treatment of the wire. In Fig. 1c (inset) in the main text, the capacitance calculated by 3D Laplace solver with a 20% reduction is plotted. These plotted capacitance values are used for mobility extraction and expected to represent channel capacitance realistically.

S4. Comparison of field effect mobility extraction methods

We extract mobility values by fitting the conductance curves $G(V_g)$ in a large gate voltage range. However, in the literature mobility is commonly extracted from a small gate voltage range where the transconductance has its maximum value (peak transconductance). This gate voltage range is typically close to the threshold voltage where the mobility is expected to be the highest. Here, we compare the field effect mobility obtained using our method – fitting the conductance curves $G(V_g)$ – to the field effect mobility obtained from peak transconductance, the standard method for extracting mobility in nanowires. We denote the mobility obtained using the latter as peak-mobility. We describe the extraction of peak-mobility in the following: By numerically differentiating the measured $G(V_g)$ shown in Fig. S1a, one obtains the transconductance $g_m = dG/dV_g$. This transconductance is shown in Fig. S1b (black curve). After taking the numerical derivative, an averaging is performed to remove the fluctuations in transconductance (red curve in Fig. S1b). The peak-mobility is then obtained from the maximum value of transconductance using $\mu = g_m L^2/C$ (see eq. 2). Peak-mobility depends strongly on the chosen averaging range. This dependence is shown in Fig. S1c. Here, mean forward peak-mobility of 11 devices from a single fabrication run is plotted against the averaging range. We choose the averaging range to be 1.8 V, the value at which the rapid decrease of peak-mobility with respect to averaging range diminishes.

Next interface resistances are taken into account since they affect the extracted peak-mobility. This is done by subtracting the contribution of a gate-independent series resistance R from the measured conductance curve $G(V_g)$. Fig. S1f shows an example of such a conductance curve corrected for interface resistances. From such a curve we determine the transconductance, and from the maximum value of transconductance peak-mobility is extracted. The peak-mobility depends on the subtracted R, shown in Fig. S1d. Here, as mentioned above, mean forward peak-mobility of 11 devices from a single fabrication run is plotted. (The peak-mobility for $R = 0$ is the one indicated with a green arrow in Fig. S1c.) For zero subtracted resistance ($R = 0$), the transconductance has a global maximum near pinch-off (Fig. S1b, red curve). Upon increasing the value of R subtracted from $G(V_g)$, the transconductance values increase for all gate voltages, with the amount of increase being larger for higher gate voltages. When R exceeds the value of interface resistances R_s, the transconductance no longer has a global maximum near pinch-off. When R is increased even further, transconductance starts to increase with gate voltage, a case we regard to be unrealistic. R_s for individual devices varies between 1.5 kΩ and 4 kΩ, with an average R_s of $\sim$ 3 kΩ. After the subtraction of R_s, the mean peak-mobility of 11 devices obtained using forward sweep direction is (27.1 $\pm$ 4.2) $\times$ 10^3 cm^2/Vs (see Fig. S1d) compared to (28.7 $\pm$ 4.8)$\times$ 10^3 cm^2/Vs obtained from fits to the conductance curves. Both values are within error margin the same. Comparing mobilities of individual devices obtained using both methods (Fig. S1e), we conclude that both methods give similar values. The small difference is due to slightly

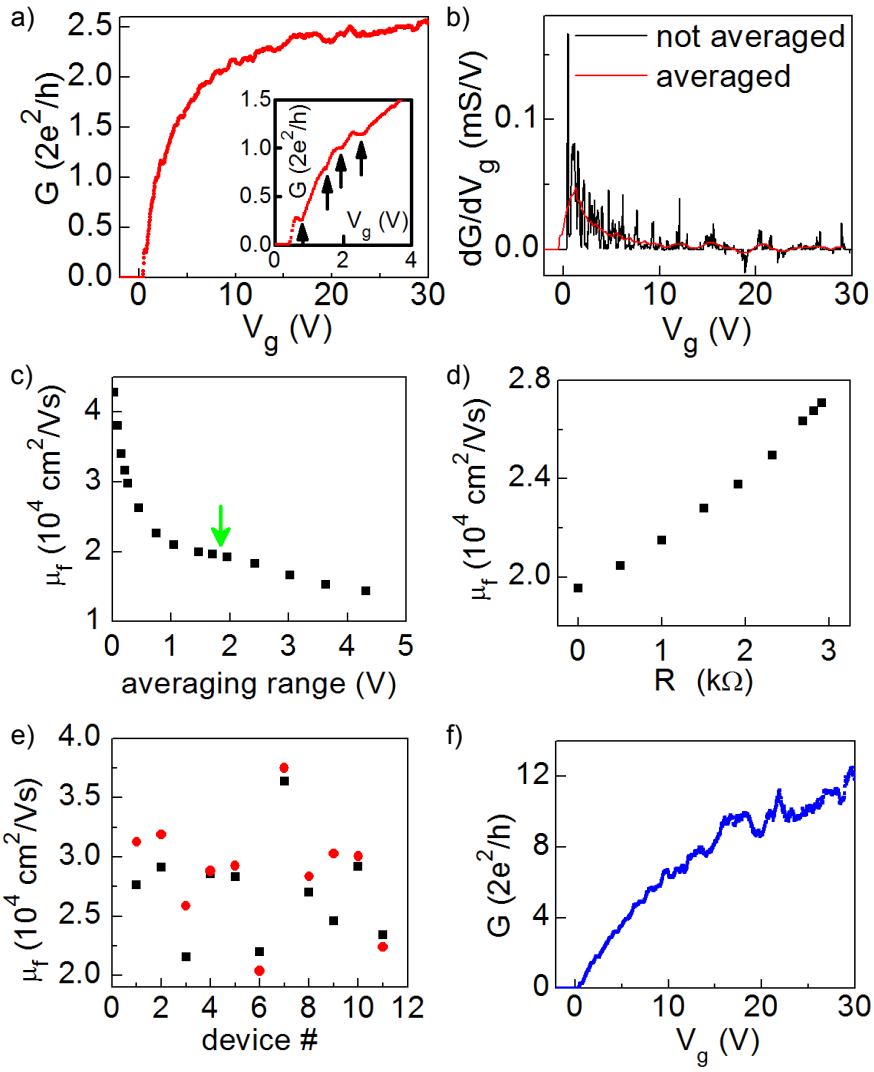

Figure S1. a) Conductance G, as a function of gate voltage V_g. Inset: Zoom-in of the conductance near pinch-off. The arrows point at universal conductance fluctuations resulting in fluctuations in transconductance. **b)** Transconductance dG/dV_g without (black) and with (red) averaging over 1.8 V gate voltage range. Averaging is applied to remove the fluctuations that lead to peaks and dips in the transconductance. **c)** Field effect mobility μ_f obtained from peak transconductance as a function of gate voltage averaging range. Plotted values of peak-mobility is the average of 11 devices on the same chip (long evacuation time experiment, Fig. 2). The green arrow denotes the averaging range of 1.8 V used for the averaged curve in panel b. This averaging window is used in further analysis to obtain peak-mobility. **d)** Peak-mobility as a function of series resistance subtracted from $G(V_g)$. Peak-mobility is the average of 11 devices on the same chip. **e)** Comparison between field effect mobility μ_f obtained for individual devices using the fit according to eq. 3 (red points) and the mobility obtained from peak transconductance (black points). **f)** Conductance as a function of gate voltage after the correction for interface resistances. For this device an interface resistance $R_s = 4$ kΩ is assumed. Conductance curve without the correction for R_s is shown in panel a.

larger interface resistances obtained from the fitting method, giving an average R_s of 3.7 kΩ.

S5. Simplification of gate voltage-independent interface resistances

Here we check our simplification of modelling the interface resistances R_s to be gate voltage independent. We fit the measured device conductance $G(V_g)$ using eq. 3 to determine R_s, the mobility μ, and the threshold voltage V_{th}. The measured device conductance after the subtraction of R_s is denoted by $G_{\mathrm{ch}}(V_g)$. In our model $G_{\mathrm{ch}}(V_g)$ has the form $G_{\mathrm{L}}(V_g) = (V_g - V_{th})\mu C/L^2$, which corresponds to a conductance linear in gate voltage with the transport properties extracted from the fit mentioned above. In Fig. S2 we plot representative curves of $G_{\mathrm{ch}}(V_g)$ (black) and compare them with $G_{\mathrm{L}}(V_g)$ (red). We find that $G_{\mathrm{L}}(V_g)$ matches well with $G_{\mathrm{ch}}(V_g)$, demonstrating that our simple model with gate voltage-independent interface resistances is a valid approximation for our measurements.

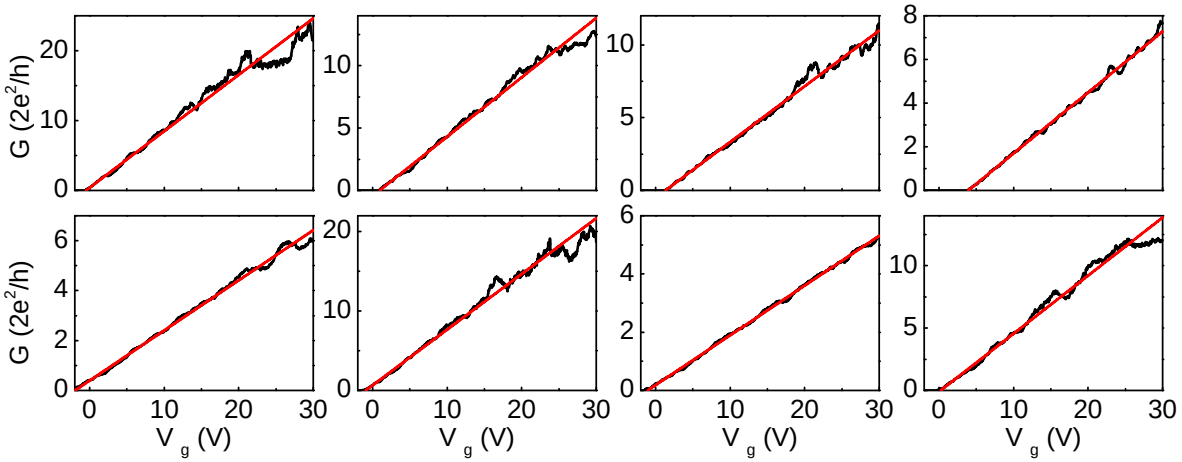

Figure S2. Panels show the measured device conductance after subtracting the interface resistance, $G_{\mathrm{ch}}(V_g)$ (black), together with $G_{\mathrm{L}}(V_g)$ (red), which is the conductance linear in gate voltage with the transport properties extracted from the fit. $G_{\mathrm{ch}}(V_g)$ shown in upper row (lower row) are from the data set presented in Fig 2a (Fig 3a) in the main text.

S6. Overview of measured devices

- Evacuation time experiment (fabricated according to our optimized recipe described above). Mobility was extracted from measurements of 11 devices with contact spacing between 1 and 2 μm. Average contact spacing 1.41 μm. Data reported in Fig. 2. Long evacuation time data is also included in Fig. 4 and Fig. 5 (Batch A).
- FETs without substrate cleaning and with long-time evacuation. Fabricated according to our optimized recipe, with the exception that we used different settings for Ar etching. Here we used 400 V on the sample holder and etched for 150 s while keeping all the other settings the same. This yields the same amount of etching of InSb nanowire ($\sim$ 70 nm) as etching at 300 V for 300 s. 11 devices, contact spacing of all devices is 2 μm. Data reported in Fig. 3.
- FETs with substrate cleaning and with long-time evacuation. Fabricated according to our optimized recipe, with the exception that we used different settings for Ar etching. Here we used 400 V on the sample holder and etched for 150 s while keeping all the other settings the same. This yields the same amount of etching of InSb nanowire ($\sim$ 70 nm) as etching at 300 V for 300 s. 11 devices, contact spacing between 1 and 2 μm. Average length 1.42 μm. Data reported in Fig. 3, Fig. 4, and Fig. 5 (Batch B).
- FETs fabricated according to our optimized recipe. 13 devices, contact spacing between 1 and 2.5 μm. Average contact spacing 1.73 μm. Data reported in Fig. 4 and Fig. 5 (Batch C).
- FETs fabricated according to the recipe, with the addition of a thin layer of perfluorodecyltrichlorosilane (FDTS) deposited onto the devices after fabrication. No improvement of mobility was observed with respect to devices without FDTS. 11 devices, contact spacing between 1 and 2.5 μm. Average contact spacing 1.64 μm. Data reported in Fig. 4.
- FETs fabricated according to our optimized recipe, but with substrate oxygen plasma cleaning of 60 s instead of 10 minutes. After oxygen plasma cleaning a thin layer of FDTS was deposited onto the substrate, after which fabrication proceeded according to the recipe. No improvement of mobility was observed with respect to devices without FDTS and with the usual 10 minutes cleaning. 10 devices, contact spacing between 1 and 2.5 μm. Average contact spacing 1.85 μm. Data reported in Fig. 4.

S7. Average device characteristics obtained from several measurement and fabrication runs

	Short-time evacuation	Long-time evacuation	Reexposed to air
μ_f (10^3 cm^2/Vs)	14.6 ± 3.0	28.7 ± 4.6	17.3 ± 2.8
μ_r (10^3 cm^2/Vs)	10.7 ± 2.1	18.6 ± 3.0	12.1 ± 1.9
μ_{avg} (10^3 cm^2/Vs)	12.7 ± 2.7	23.7 ± 3.6	14.7 ± 2.2
V_{th} (V)	1.70 ± 0.29	-0.20 ± 0.36	1.96 ± 0.43
V_{hyst} (V)	2.75 ± 0.47	1.31 ± 0.30	2.40 ± 0.36
R_s ($k\Omega$)	3.7 ± 0.7	3.7 ± 1.0	4.1 ± 1.2

Table S1. Mobility, threshold voltages V_{th}, hysteresis, V_{hyst} and series resistances, R_s, extracted from fits to conductance curves $G(V_g)$ of the evacuation time experiment. Mobility is obtained with forward sweep direction, μ_f and reverse sweep direction, μ_r. The average mobility of these two sweep directions, μ_{avg}, is also reported. V_{th} is the threshold voltage obtained from fits to $G(V_g)$ taken with forward sweep direction. Mobility, threshold voltage and hysteresis are also shown in Fig. 2c, d and e, respectively.

Batch	A	B	C
μ_f (10^3 cm^2/Vs)	28.7 ± 4.6	28.9 ± 4.4	26.0 ± 4.7
μ_r (10^3 cm^2/Vs)	18.6 ± 3.0	19.4 ± 3.9	16.4 ± 3.0
μ_{avg} (10^3 cm^2/Vs)	23.7 ± 3.6	24.2 ± 3.9	21.2 ± 3.8
V_{th} (V)	-0.20 ± 0.36	-0.51 ± 0.45	-0.37 ± 0.39
V_{hyst} (V)	1.31 ± 0.30	1.14 ± 0.22	1.41 ± 0.28
R_s ($k\Omega$)	3.7 ± 1.0	3.0 ± 0.8	4.8 ± 1.8

Table S2. Mobility, threshold voltage, V_{th}, hysteresis, V_{hyst}, and series resistance, R_s, obtained from fits to the conductance curves $G(V_g)$ of three batches of high-mobility devices. Mobility is obtained with forward sweep direction, μ_f and reverse sweep direction, μ_r. The average mobility of these two sweep directions, μ_{avg}, is also reported. V_{th} is the threshold voltage obtained from fits to $G(V_g)$ taken using forward sweep direction. Mobilities and series resistances are also shown in Fig. 5.