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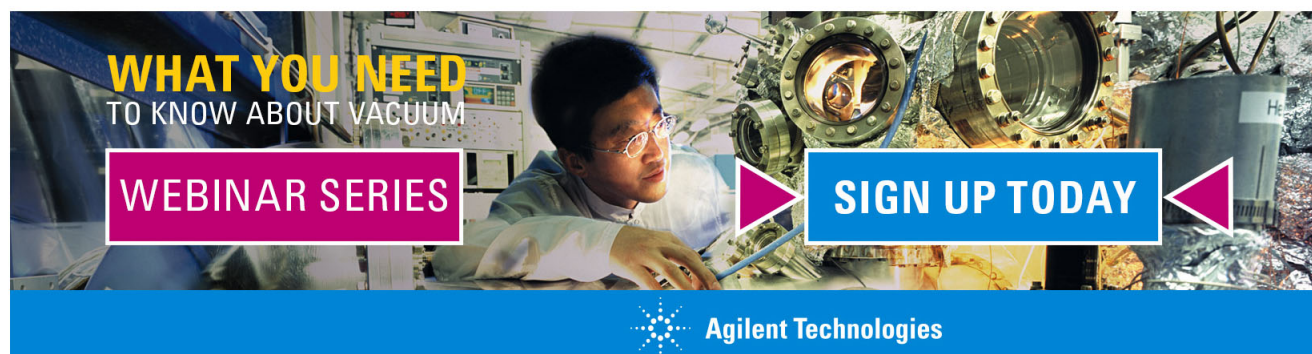Appl. Phys. Lett. **81**, 1833 (2002); 10.1063/1.1504882

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Gate-tunable high mobility remote-doped InSb/In$_{1-x}$Al$_x$Sb quantum well heterostructures

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Gate-tunable high-mobility InSb/In$_{1-x}$Al$_x$Sb quantum wells (QWs) grown on GaAs substrates are reported. The QW two-dimensional electron gas (2DEG) channel mobility in excess of 200 000 cm^2/V s is measured at T = 1.8 K. In asymmetrically remote-doped samples with an HfO$_2$ gate dielectric formed by atomic layer deposition, parallel conduction is eliminated and complete 2DEG channel depletion is reached with minimal hysteresis in gate bias response of the 2DEG electron density. The integer quantum Hall effect with Landau level filling factor down to 1 is observed. A high-transparency non-alloyed Ohmic contact to the 2DEG with contact resistance below 1 Ω·mm is achieved at 1.8 K. © 2015 AIP Publishing LLC.
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InSb has the smallest electron effective mass ($m* = 0.014\,m_e$) and the largest known room-temperature bulk electron mobility of 78 000 cm^2/V s of any semiconductor, making it appealing as a channel material in heterostructure transistors (HEMT, HBT) that can operate at higher frequency and lower voltage than GaAs and InP based devices.[1] The strong spin-orbit interaction and a giant g factor (-51 in bulk InSb) makes InSb an interesting candidate for potential exploitation in spintronics[2] or topological quantum computing using non-Abelian Majorana fermions.[3,4] In fact, signatures of Majorana fermions were first reported in solid state systems using a gated InSb nanowire-superconductor hybrid device.[5–7] However, integration of bottom-up nanowires remains a difficult task. To scale to more complicated structures for topological qubits, an alternative approach is to fabricate InSb nanowires and "T" junctions by top-down techniques starting from planar epitaxial heterostructures. Electron mobility greater than 100 000 cm^2/V s and a corresponding electron mean-free path in the sub-micrometer range are achievable. Although InSb/InAlSb quantum wells (QWs) with two-dimensional electron gas (2DEG) mobility in excess of 200 000 cm^2/V s have been developed,[8,9] they are often plagued with parallel conduction channels which may be difficult to deplete. Gate tunability of the 2DEG density to full depletion is needed in split-gate quantum structures. However, making gated devices for InSb-based materials has been a major challenge. Schottky barrier gates to such narrow-gap materials are leaky due to the low barrier

height.[10] For metal-oxide-semiconductor (MOS) structures, previous studies found difficulties in growing high-quality gate dielectrics with appropriate interface properties to achieve depletion without hole accumulation or large hysteresis.[11–14] So far only one work claimed complete 2DEG channel depletion on InSb MOS device, with the 2DEG mobility reaching $\sim$70 000 cm^2/V s (at a 2DEG density of $\sim 3.3 \times 10^{11}$ cm^{-2}). However, no data in the pinch-off regime was reported.[14] In this letter, we show that all the aforementioned challenges can be overcome with carefully designed epitaxial growth and device processing.

Previous studies showed that for remote-doped InSb/InAlSb QWs grown on lattice-mismatched GaAs substrates with typical rms surface roughness of the order of a few monolayers, the contribution of interface roughness scattering has a strong dependence on the well width and is negligible for a QW thickness of 30 nm or greater. The low-temperature InSb 2DEG mobility is limited by remote ionized impurity (RII) scattering originating from ionized dopants (e.g., Te or Si) in the δ-doping layer and charged defects in the buffer layer.[9] Screening by electrons in both the QW and the δ-doping plane improves the mobility. However, electrons in the δ-doping plane and higher subbands in the QW act as parallel conduction channels and are undesirable for certain device operations that require a single electron channel, e.g., the quantum Hall effect (QHE). Magnetotransport of a Hall device is well suited to diagnose the parallel conduction. In the absence of parallel conduction, a clean QHE with the longitudinal resistance showing zero-resistance states and quantized plateaus in Hall resistance should be observed. Otherwise, the magnetoresistance oscillations are superimposed on a background of parallel conduction and never become zero (see Refs. 15 and 16). Due to the rather low

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conduction band offsets in InSb/InAlSb QWs, the maximum 2DEG density that can be achieved without introducing parallel conduction is typically less than $\sim 4 \times 10^{11}$ cm^{-2}.[17] Inserting multiple doping layers with a goal of increasing the 2DEG density can produce undesirable parallel conduction channels. We have prepared and measured both symmetrically doped InSb QWs (with n-type doping layers at both above and below the QW) and asymmetrically doped QWs (i.e., with only n-type doping layer(s) above the QW). We found that the 2DEG density in a symmetrically doped QW is nearly doubled as compared with an asymmetrically doped QW. However, the parallel conduction in the bottom doping layer cannot be eliminated without first depleting the 2DEG channel. In contrast, asymmetrically doped samples do not have such issues. Therefore, in this work, we focus on results from asymmetrically doped samples. We report that by optimizing the design, epitaxial growth, and fabrication process, an asymmetrically doped InSb/InAlSb QW can achieve both 2DEG mobility higher than 200 000 cm^2/V s and a nearly hysteresis-free gate bias response to full depletion.

Fig. 1 shows the schematic diagram of the heterostructure growth and gated Hall device design used in this work. Samples were grown in a Varian Gen II molecular beam epitaxy (MBE) system equipped with valved crackers for As, Sb and effusion cells for Ga, In, and Al. The InSb/InAlSb single QW heterostructure (Fig. 1(a)) was grown on a semi-insulating GaAs (100) substrate, on top of a GaAs buffer, an AlSb nucleation layer, and a 4 μm thick strain-relaxed In$_{1-x}$Al$_x$Sb buffer layer (x = 8%). The InSb QW thickness (30 nm), the Si δ-doping level (5×10^{11}cm^{-2}–1×10^{12} cm^{-2}) and the distance d to the QW (20 nm) were selected after several rounds of test growths and Schrödinger-Poisson (SP) simulations to achieve high 2DEG mobility. The surface depth of the Si δ-doping was in the range of 20–50 nm (20 nm used for the data presented). Transmission electron microscopy (TEM) of the sample cross sections (Fig. S1 in Ref. 15) showed that the defective region extends to about 3 μm into the In$_{1-x}$Al$_x$Sb buffer layer and the buffer region beyond that thickness has relatively low density of dislocations. To inspect the effect of buffer thickness, we grew several samples with identical layer structures and growth conditions, except that the buffer thickness was changed to either 1 μm or 6 μm. For 1 μm-buffer samples, the low-temperature 2DEG mobilities dropped from $\sim$200 000 cm^2/V s to $\sim$60 000 cm^2/V s, whereas for 6 μm-buffer samples the mobility improvement over 4 μm-buffer samples was

marginal. The rms surface roughness of the as-grown sample surface is 1.3 nm for 1 μm-buffer samples and 1.9 nm for 4 μm-buffer samples over an area of 10 μm $\times$ 10 μm.[15]

Processing of narrow-gap InSb-based materials poses another major challenge. At elevated process temperatures, several mechanisms can deteriorate the device characteristics, including, but not limited to, interface roughening, preferential evaporation of Sb atoms on exposed surfaces, and diffusion of In and Sb into gate dielectrics.[18] As a precaution, we have kept the process thermal budget conservatively at or below 180 °C. For high-frequency transistors and superconductor-semiconductor hybrid quantum devices, a low resistance Ohmic contact to the InSb 2DEG is desired for various reasons. Conventional Ohmic contacts on the top surface by eutectic alloys such as AuGe/Ni or AuGe/Pt[19] require a post-deposition anneal, which may cause material damage and surface leakage. Instead, we took the approach of etching to the InSb QW using an Ar ion etch with secondary ion end-point detection followed by non-alloyed Ti/Au evaporation (500 Å Ti/3000 Å Au). The contact resistance is characterized by a transmission line method and is found to be less than 1 Ω·mm at both room temperature and low temperatures.[15]

For fabricating gated MOS devices, a major challenge is growing high-quality gate dielectrics on (Al)InSb with low gate leakage. It was reported that the typical interface trap density D_{it} for Al$_2$O$_3$ gate oxide by atomic layer deposition (ALD) was in the range of 1.1×10^{12} cm^{-2}eV^{-1} to 1.7×10^{13} cm^{-2}eV^{-1}, and the gate depletion and hysteresis was improved by replacing the InSb surface layer with a larger bandgap Al$_{0.1}$In$_{0.9}$Sb.[14] ALD HfO$_2$ was shown to be a superior diffusion barrier than ALD Al$_2$O$_3$ for InSb.[18] Another advantage of ALD HfO$_2$ is its much larger dielectric constant ($\kappa \sim$ 18–21) than ALD Al$_2$O$_3$ ($\kappa \sim$ 7–9). We deposited a 20–40 nm high-κ ALD HfO$_2$ thin film as the gate dielectric using remote plasma enhanced ALD (PEALD) at a low substrate temperature of 175 °C. PEALD is expected to reduce impurities and increase the film density as compared with thermal ALD process. A dielectric breakdown field of $\sim$3 MV/cm was measured at room temperature.

For magnetotransport characterizations, materials were processed into 6-lead Hall bars using standard photolithography techniques. Hall bar mesas (200 μm long, 20 μm wide) with Hall voltage lead spacing of 100 μm were wet etched using citric-acid based solution (see Refs. 15 and 20). A top view micrograph of an actual device is shown in Fig. 1(b) with a schematic cross section shown in Fig. 1(c). Processed devices were tested at 1.7–1.8 K in a Lakeshore 9709A Hall measurement system equipped with a 9 T magnet using AC lock-in technique (frequency at 9 Hz and time constant at 30 ms). The drain/source of the Hall bar were connected in series with a 25 kΩ load resistor under a 10 mV AC bias, which restricts the channel current to below 400 nA to avoid localized Joule heating. Measured gate leakage was at or below the noise floor of the instrument ($\sim$20 pA) for all DC biases applied (up to $\pm$5 V).

The field dependent magnetoresistance R$_{xx}$ and Hall resistance R$_{xy}$ allow for extraction of carrier mobility and sheet charge density. The linearity of R$_{xy}$ vs. B (not shown) suggests that single B field measurement is adequate. Fig. 2
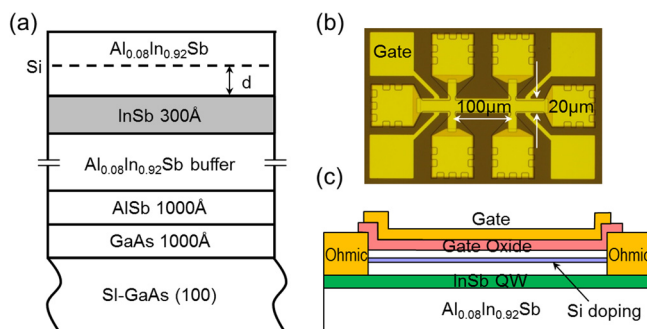

FIG. 1. (a) Schematic diagram of the heterostructure growth, (b) photograph of a gated Hall bar device, (c) schematic cross section of the Hall bar device.
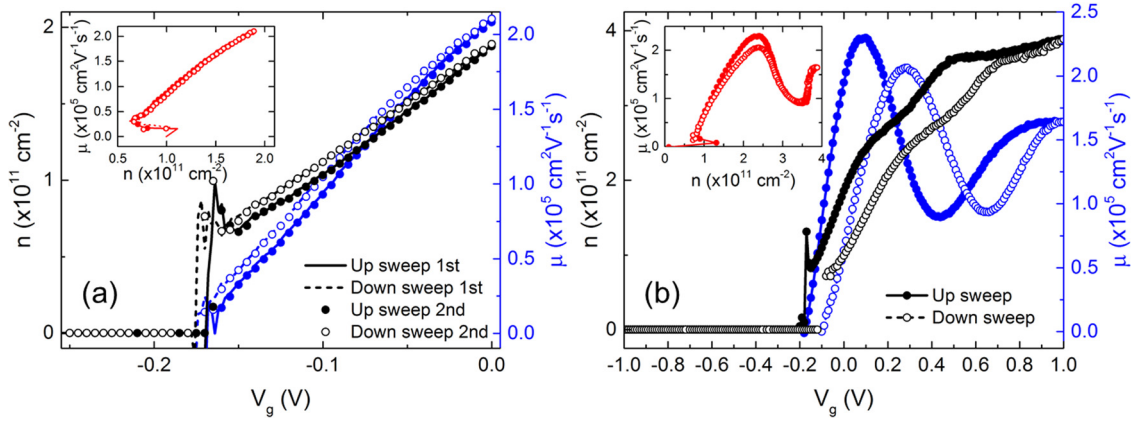
FIG. 2. Electron density and mobility of the InSb 2DEG as a function of gate bias V_g measured at B = 0.1 T (low field). (a) Depletion-mode gate bias double sweeps (0 V to −0.3 V then back to 0 V, repeated twice). (b) Wide-range bipolar gate bias double sweeps (−1 V to 1 V then back to −1 V) of the same device. Insets show the mobility vs. electron density.

shows the electron density and mobility of the InSb 2DEG as a function of gate bias, V_g, measured at B = 0.1 T (low field). In Fig. 2(a), repeated negative Vg double sweeps (0 V to −0.3 V then back to 0 V) were applied to a Hall bar to deplete/replenish the 2DEG channel. A small hysteresis of ∼20 mV was seen in the initial gate bias sweep after the Hall device was cooled to 1.8 K with all the electrical contacts grounded (data not shown). In all subsequent sweeps, the hysteresis was reduced to only ∼10 mV and remained the same irrespective of the voltage sweep rate. The mobility vs. sheet charge density (Fig. 2(a) inset) follows a linear dependence, which suggests that carrier scattering is dominated by the interplay of remote dopants and background impurities. The 2DEG channel is completely pinched off at a small negative gate bias of V_P = −0.17 V (V_P varies slightly from device to device and is in the −0.1 V to −0.25 V range). The channel pinch-off always occurs abruptly when the 2DEG electron density drops below certain thresholds (2 to 6×10^{10} cm^{-2}, varies with device), suggesting a percolation type of behavior with a minimum electron density for the metal-insulator transition to occur.[21] No sign of hole accumulation was observed in samples using a top Si δ-doping level of 1×10^{12} cm^{-2}. However, hole accumulation was observed in samples using a lower Si doping level of 5×10^{11} cm^{-2}.[15] This suggests that a potential barrier in the valence band produced by the δ-doping layer is important in preventing hole accumulation towards the surface, which requires further investigation.

The situation is different when a positive gate bias sweep is used. In Fig. 2(b), bipolar wide-range gate bias double sweeps (−1 V to 1 V then back to −1 V) were applied to the same Hall device. Electron density in the 2DEG channel keeps increasing at higher positive biases, while mobility peaks at 230 000 cm^2/V s at V_g = 0.1 V then drops at higher gate biases, with a corresponding decrease in the slope of n-V_g. Both can be explained by the onset of filling into the 2nd subband which has a lower mobility due to hybridization with the δ-doping layer, as shown by SP simulation (see Fig. 3). The 2DEG channel turn-on threshold shifts to a larger value after positive V_g sweeps and a much larger hysteresis is produced accordingly. However, the μ vs. n relationship is still consistent with low hysteresis (Fig. 2(b) inset).

The slope of n-V_g can be used to estimate the interface trap density using an equivalent circuit capacitor model of

$$dn/dV_g = C_{tot}/e[1 + C_{it}(C_{SC} + C_{2D})/(C_{SC}C_{2D})]$$

in the absence of parallel conduction and hole accumulation.[14] Here, $C_{it} = e^2 D_{it}$ is the capacitance associated with interface traps. C_{ox} and C_{sc} are the capacitance per unit area
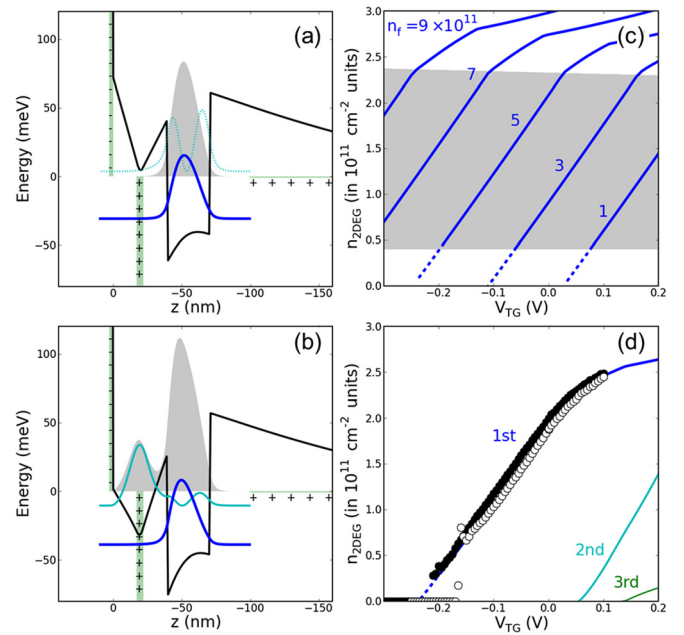

FIG. 3. Self-consistent Schrödinger-Poisson simulations of the top-doped structure. (a) Conduction band diagram (CBD) at V_g = 0 when only a single channel (the QW first subband) is populated. Mobile charge density is shown as shaded area. Position of the intentional top Si doping (n_f = 5 × 10^{11} cm^{-2}) along with that of the weakly V_g-dependent dielectric interface charge density (for D_{it} = 7.5 × 10^{11} cm^{-2} eV^{-1}, total $n_{Surface}$ ∼ −8 × 10^{11} cm^{-2}) and a weak intrinsic bulk doping (n_{Bulk} = 1 × 10^{15} cm^{-3}) are depicted schematically. Envelope function density for electron states at the bottom of the first and second subbands are shown by solid (blue) and dotted (cyan) lines, respectively. (b) CBD at V_g = 0.15 V, wherein two channels—one in the QW and one in the doping layer—are populated appreciably. (c) First channel charge density as a function of the fixed charge density n_f in the doping layer. Shaded region depicts the desired single channel regime. (d) Mobile charge density (channel-partitioned) vs top gate bias. Experimental data for two different devices are shown by solid and open circles.
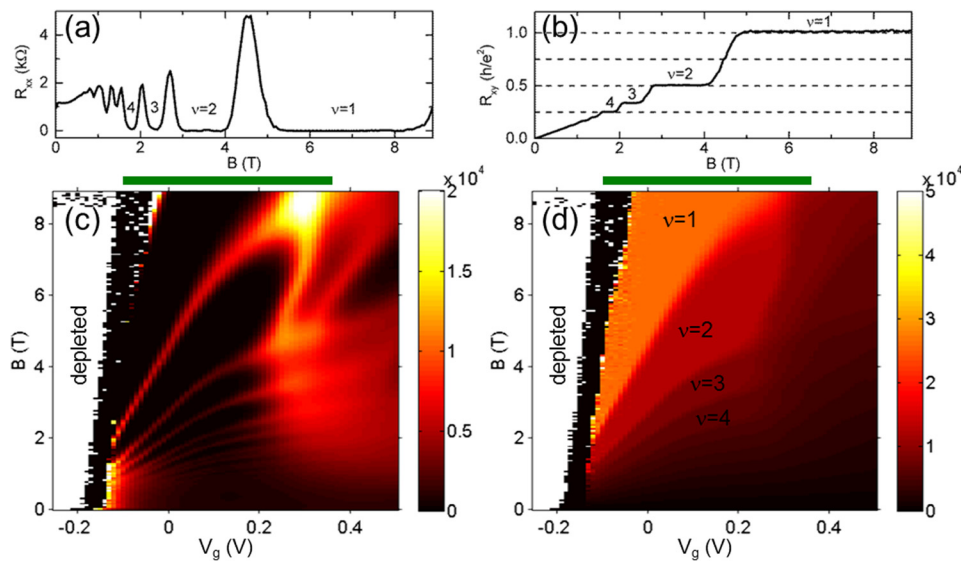
FIG. 4. Field dependent (a) magneto resistance R_{xx} and (b) Hall resistance R_{xy} at $V_g = 0$ V. 2D maps of (c) R_{xx} and (d) R_{xy} for all B fields (0–8.9 T) and gate biases (−0.25 to 0.5 V). Green bars show the regime wherein electron mobility of the InSb 2DEG is greater than 100 000 cm^2/V s.

of the HfO$_2$ ($\kappa = 18.5$) and the semiconductor layers above the QW ($\kappa = 16.4$), $C_{2D} = e^2 m^* / \pi \hbar^2$ is the quantum capacitance of the 2DEG,[22] C_{tot} is the total capacitance of C_{ox}, C_{sc}, C_{it}, and C_{2D}. In negative V_g sweeps (Fig. 2(a)), the D_{it} value of 7.5×10^{11} cm^{-2}eV^{-1} is estimated from the n-V_g slope of 8.4×10^{11} cm^{-2}/V. This D_{it} level in depletion-mode is close to a reported mean D_{it} value of 8×10^{11} cm^{-2}eV^{-1} in HfO$_2$/InSb MOS capacitors,[18] and is lower than a reported D_{it} value of 1.1×10^{12} cm^{-2}eV^{-1} in Al$_2$O$_3$/InSb devices.[14] In positive V_g sweeps (Fig. 2(b)), D_{it} levels of 1.5×10^{12} cm^{-2}eV^{-1} and 3.3×10^{12} cm^{-2}eV^{-1} are estimated from the n-V_g slopes of 7.3×10^{11} cm^{-2}/V and 5.5×10^{11} cm^{-2}/V for up and down sweeps, respectively. The large increase in D_{it} under positive gate bias sweeps indicates filling of empty interface traps towards the conduction band as electrons tunnel from the QW into the surface under positive V_g. This adds negative interface charges and shifts the 2DEG turn-on threshold higher. It is also noteworthy that our PEALD process consistently produced negative pinch-off thresholds. For devices with pinch-off voltage near −0.2 V, the 2DEG mobility already reaches 200 000 cm^2/V s at zero gate bias. Therefore, a positive gate bias sweep is not needed in depletion mode operation and electron injection can be avoided. To overcome the issue of electron injection under positive gate bias, a higher Al-content barrier can be used above the QW to reduce the electron tunneling across the InSb/InAlSb interface.

Better understanding of the self-consistent steady-state charge distribution and formation of the mobile channels in the top-gate biased structure has been achieved by employing SP simulations. Electron spatial quantization and Thomas-Fermi filling of the resulting 2D subbands are described in the effective mass approximation, accounting for the conduction band non-parabolicity (which is prominent in narrow-gap materials like InSb). Material parameters for InAlSb alloy-based heterostructures can be found in Ref. 23. Subplots (a) and (b) of Fig. 3 provide examples of the conduction band profile at two distinct gate biases ($V_g = 0$ and 0.15 V here, with an activated top Si doping level of $n_f = 5 \times 10^{11}$ cm^{-2}), allowing substantial electron density (shown as shaded area) accumulation in only a single conducting channel or two parallel channels, respectively.

Electrons in the first channel are always strongly localized in the QW (envelope function density at the bottom of the first subband is sketched by the blue line). Simulations suggest that electrons in the emerging second channel experience strong hybridization between states in the doping layer and the QW second subband (cyan line) and thus are expected to have lower mobility. The amount of fixed charge in the doping layer (due to different dose and/or fraction of activated dopants) is not fully known and would require extensive additional characterization. In Fig. 3(c), charge density in the first channel is shown as a function of the top gate bias for a set of n_f values which is treated here as a free input parameter. Its main effect is a parallel shift of gate biases that would be required to bring the structure to a similar charge distribution (even identical when no mobile charges are present above the QW). Kinks mark sequential activation of additional channels. Dashes mark the approximate low threshold for metal insulator transition.

Results of the simulations at $n_f = 5 \times 10^{11}$ cm^{-2} are compared with experimental n-V_g Hall data for two devices in Fig. 3(d), where electron density is explicitly partitioned between channels. Below $V_g \sim 0.05$ V, only a single conduction channel is present and correspondence between simulation and experiment is good all the way down to the channel pinch-off observed at n_{2DEG} of a few 10^{10} cm^{-2}.

After establishing gate tunability of the 2DEG density to full depletion with minimal hysteresis, we performed Hall measurements at high B field to examine the existence of a parasitic conduction channel, which is a common issue for InSb based narrow-gap heterostructures. High B field sweeps manifest no sign of parallel conduction between the 2DEG channel pinch off and the mobility peak (at $V_g = 0.08$ V) resulting in a clearly observable QHE. The Hall resistance shows well-defined quantized plateaus with a Landau level filling factor down to 1 and correspondingly dissipation-less zero-resistance edge states in magnetoresistance, as shown in Figs. 4(a)–4(d). For most of the QHE regime, the low-field mobility of 2DEG channel is greater than 100 000 cm^2/V s (green bars in Figs. 4(c) and 4(d)).

In conclusion, we have demonstrated efficient gate control and full depletion of high mobility InSb/InAlSb quantum

wells grown on GaAs substrates. A high-κ PEALD HfO$_2$ dielectric forms an excellent interface with InAlSb and delivers nearly hysteresis-free gate response at very low operating voltages. Combined with a 2DEG mobility greater than $100\,000\,\text{cm}^2/\text{V}\,\text{s}$ in most of the QHE regime and a low Ohmic contact resistance of less than 1 $\Omega\cdot$mm, this development facilitates fabricating top-down InSb-based nanostructures suitable for spin and Majorana fermion based quantum computation schemes.

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