

Hard superconducting gap in InSb nanowires

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Abstract

Topological superconductivity is a state of matter that can host Majorana modes, the building blocks of a topological quantum computer. Many experimental platforms predicted to show such a topological state rely on proximity-induced superconductivity. However, accessing the topological properties requires a hard induced superconducting gap, which is challenging to achieve for most material systems. We systematically studied how the interface between an InSb semiconductor nanowire and a NbTiN superconductor affects the induced superconducting properties. We step by step improve the homogeneity of the interface while ensuring a barrier-free electrical contact to the superconductor, and obtain a hard gap in the InSb nanowire. Magnetic field stability of NbTiN allows the InSb nanowire to maintain a hard gap and a supercurrent in the presence of magnetic fields (~ 0.5 Tesla), a requirement for topological superconductivity in one-dimensional systems. Our study provides a guideline to induce superconductivity in various experimental platforms such as semiconductor nanowires, two dimensional electron gases and topological insulators, and holds relevance for topological superconductivity and quantum computation.

A topological superconductor can host non-Abelian excitations, the so-called Majorana modes forming the basis of topological quantum computation.^{1–6} Both the non-Abelian property and the topological protection of Majoranas crucially rely on the energy gap provided by the superconducting pairing of electrons separating the ground state from the rest of the excitations. For most material systems that can support such a topological state, pairing is artificially induced by proximity, where the host material is coupled to a superconductor in a hybrid device geometry.^{7–27} Accessing the topological properties in hybrid devices requires a negligible density of states within the induced superconducting gap, *i.e.*, a hard induced gap, which can be attained by a homogeneous and barrier-free interface to the superconductor.^{28–32} However, achieving such interfaces remains an outstanding challenge for many material systems, constituting a major bottleneck for topological superconductivity. Here we engineer a high-quality interface between semiconducting InSb nanowires and superconducting NbTiN resulting in a hard induced gap by improving the

homogeneity of the hybrid interface while ensuring a barrier-free electrical contact to the superconductor. Our transport studies and materials characterization demonstrate that surface cleaning dictates the structural and electronic properties of the InSb nanowires, and determines the induced superconductivity together with the wetting of the superconductor on the nanowire surface. We finally show that both the induced gap and the supercurrent in the nanowire withstands magnetic fields (~ 0.5 Tesla), a requirement for topological superconductivity in one-dimensional systems.

InSb nanowires have emerged as a promising platform for topological superconductivity^{7,10,11,15,16} owing to a large spin-orbit coupling,^{33,34} a large g factor,^{35,36} and a high mobility,^{36–39} the necessary ingredients to maintain a finite topological gap in one dimension along with a high-quality interface to a superconductor resilient to magnetic fields.^{4,5,40,41} The interface quality can be inferred using tunneling spectroscopy which resolves the induced superconducting gap for a tunnel barrier away from the interface. So far spectroscopy studies on InSb nanowires attached to superconductors have reported a significant density of states within the superconducting gap, a so-called soft gap, suggesting an inhomogeneous interface.^{7,10,11,16} These subgap states invalidate the topological protection by allowing excitations with arbitrarily small energy. Soft gaps have been observed also in other hybrid systems for cases where tunneling spectroscopy is applicable.^{8,12,42,43} For other cases, interface inhomogeneity is indirectly inferred from a decreased excess current or supercurrent due to a deviation from Andreev transport,⁴⁴ a common observation in hybrid systems.^{17,18,24} Exceptions are the InAs-Al materials combination for which an epitaxial interface to the superconductor has recently been synthesized resulting in a hard gap,^{29–32} along with Bi₂Se₃¹⁹ and Bi₂Te₃^{20,21} epitaxially grown on a superconducting NbSe₂ substrate. However these studies do not provide further insight into the soft gap problem in material systems for which either epitaxy remains a challenge or when a high structural quality does not guarantee a barrier-free interface (*e.g.* due to carrier depletion). Here we tackle the soft gap problem in InSb nanowire devices by focusing on the constituents of a hybrid device realization which are crucial for the interface.

In general, realizing a hybrid device begins with surface preparation of the host material followed by the deposition of a superconductor. Surface preparation ensures a barrier-free coupling

to the superconductor and is of paramount importance for host materials with low surface electron density or a small number of electronic subbands (*e.g.* semiconductor nanowires). Here we also adopt this procedure for our nanowires⁴⁵ whose native surface oxide forms an insulating layer that has to be removed. We describe the details of the nanowire growth, fabrication, and measurement setup in Supporting Information. Fig 1a and b show a completed device with two lithographically defined superconducting electrodes having a small separation (~ 150 nm) on an InSb nanowire. A degenerately doped silicon substrate acts as a global back gate, tuning the carrier density in the wire. The small electrode separation allows us to electrostatically define a tunnel barrier in the wire section between the electrodes by applying negative gate voltages. Fig 1c and e show the induced gaps measured by tunneling spectroscopy for two common realizations of an InSb nanowire hybrid device. For the device in Fig 1c, a sulfur-based solution⁴⁶ is used to clean the wire surface followed by evaporation of Ti/Al with Ti the wetting layer, whereas Fig 1e is from a device for which the wire surface is *in-situ* cleaned using an argon plasma followed by sputtering of NbTiN. Fig 1d shows the conductance traces of the sulfur-Ti/Al device indicating a hard induced gap $2\Delta \sim 0.3$ meV for low gate voltages when decreased transmission suppresses Andreev reflection. In contrast, Fig 1f demonstrates that the argon-NbTiN device shows a soft induced gap even for the lowest gate voltages, but with a gap $2\Delta \sim 1$ meV inherited from NbTiN, a superconductor with a large gap and high critical field. Both device realizations present a challenge towards topological protection. In the first case, a magnetic field (~ 0.5 T) to drive the wire into the topological state destroys the superconductivity of Al (Supporting Fig 1). Al can withstand such fields when it is very thin (< 10 nm) in the field plane, however, such thin Al films contacting a nanowire have so far only been achieved by epitaxy.^{13,14,30} In the second case, the subgap states render the topological properties experimentally inaccessible.

We now turn our attention to the surface of InSb nanowires prior to superconductor deposition. To determine the effects of surface cleaning on transport, we characterized long-channel nanowire devices with ~ 1 μm electrode separation whose channel surface is cleaned using different methods, along with control devices with pristine channels (details in Supporting Information). Fig

2 shows the measured conductance as a function of gate voltage with the traces representing an average over different devices and the shades indicating the standard deviation. We find that the argon-cleaned channel behaves strikingly different than sulfur-cleaned and pristine channels: First, the argon-cleaned channel does not pinch off, showing a finite conductance even for lowest gate voltages, indicating a deviation from a semiconducting gate response. Second, it shows a lower transconductance $\propto dG/dV_{\text{gate}}$ compared to sulfur-cleaned and pristine channels indicating a low mobility. These observations are consistent with previously reported formation of metallic In islands on the InSb surface after argon cleaning.⁴⁷ In contrast, the sulfur-cleaned channel shows a gate response similar to the pristine channel apart from a shift of the threshold voltage towards negative values. This behaviour indicates a surface electron accumulation expected for III-V semiconductors treated with sulfur-based solutions.^{48–50} A close inspection of the cleaned channels reveals the differences in nanowire surface morphology after argon and sulfur cleaning (Fig 2 inset). While argon cleaning created a roughness easily discernible under high-resolution electron microscope for different plasma parameters, we find that sulfur cleaning, which removes ~ 5 nm of the wire, leaves a smoother InSb surface. TEM studies on the cleaned wire surface confirm this observation (Supporting Fig 2). We finally note that argon cleaning (when used for removing the nanowire native oxide to realize electrodes, *e.g.* in Fig 1e,f) gave contact resistances comparable to those obtained by sulfur cleaning for an argon plasma significantly etching the nanowire surface (> 15 nm). This indicates that a complete removal of the native oxide (~ 3 nm) does not guarantee a barrier-free interface to the superconductor for InSb nanowires, which could be related to the surface depletion of InSb previously reported for a (110) surface,⁵¹ the orientation of our nanowire facets. In the rest of the Letter we use sulfur cleaning to remove the native oxide on the nanowire surface prior to superconductor deposition.

Next, we investigate the wetting of the superconductor on the nanowire surface. Fig 3a shows the conductance averaged over different nanowire devices realized with and without a thin layer of NbTi (5 nm), a reactive metal deposited right before NbTiN to ensure its wetting on the wire. Inclusion of a NbTi wetting layer provides a substantial improvement in contact resistance, allow-

ing to resolve five quantized plateaus in ensemble-averaged conductance. Tunneling spectroscopy (Fig 3b-d) reveals the differences in superconducting properties of the devices with and without the wetting layer. Fig 3b shows an induced gap $2\Delta \sim 1$ meV for a device with NbTi wetting layer. Low gate voltages bring the device into the tunneling regime revealing a hard induced gap, shown in Fig 3c. In contrast, Fig 3d and e show that omitting the wetting layer results in poor induced superconductivity with no clearly identifiable gap and a tunneling conductance dominated by Coulomb blockade with irregular diamonds. Finally, to verify the importance of the wetting of the superconductor on the wire surface we realized InSb-Al nanowire devices without a Ti wetting layer. These devices also showed very high contact resistances, while inclusion of Ti wetting layer gave low contact resistances and a finite supercurrent (Supporting Fig 3), in addition to a hard induced gap shown in Fig 1c and d.

We note that the devices with NbTi/NbTiN electrodes in Fig 3 did not show a supercurrent, a requirement for a nanowire-based topological quantum bit,^{52–55} which we attribute to a residual interface barrier effective at small bias. This could be related to the *ex-situ* nature of sulfur cleaning, leaving the wire surface exposed to ambient which cannot exclude adsorbents at the interface. To improve the small bias response of our devices we included an *in-situ* argon cleaning of sufficiently low-power to avoid a damage to the InSb nanowire surface. Indeed, after a low-power argon cleaning we find a high yield of devices showing a finite supercurrent measured at 250 mK (Supporting Fig 4). For another chip with 18 nanowire devices but measured at 50 mK, we find a clear supercurrent for all devices (Supporting Fig 5) while obtaining an induced gap $2\Delta \sim 1$ meV or larger (Supporting Fig 6 and 7).

We now turn to the magnetic field response of hybrid devices realized with sulfur cleaning followed by an *in-situ* low-power argon cleaning, and NbTi/NbTiN superconducting electrodes. Fig 4a and b show the differential conductance for varying gate voltages at zero magnetic field measured at 50 mK (details in Supporting Fig 6). We find a hard induced gap $2\Delta \sim 1.5$ meV which confirms the noninvasiveness of our low-power cleaning. We then choose a gate voltage where the device is in the tunneling regime (orange trace in Fig 4b) and perform spectroscopy for increasing

magnetic fields along the wire axis, shown in Fig 4c. In Fig 4d we plot the conductance traces taken at different magnetic fields showing an induced gap which remains hard up to ~ 0.5 T. Increasing fields decrease the induced gap size and increase the subgap conductance but a gap feature can be identified up to 2 T revealing the large critical field of NbTiN. Fig 4e shows the critical current of another device (details in Supporting Fig 7) measured at a large gate voltage when the nanowire is highly conducting. In Fig 4f we plot the current-voltage traces for different magnetic fields. We find a critical current of ~ 40 nA at zero magnetic field which remains finite up to at least 1 T.

In conclusion, we demonstrated a hard induced gap and supercurrent in InSb nanowires in the presence of magnetic fields (~ 0.5 Tesla) owing to a high-quality interface to NbTiN engineered using a noninvasive nanowire surface cleaning and by including a wetting layer between the nanowire and the superconductor, which together ensure a homogeneous and barrier-free coupling to the superconductor. Our results provide a guideline for inducing superconductivity in semiconductor nanowires, two dimensional electron gases and topological insulators, and hold relevance for topological superconductivity in various material systems.

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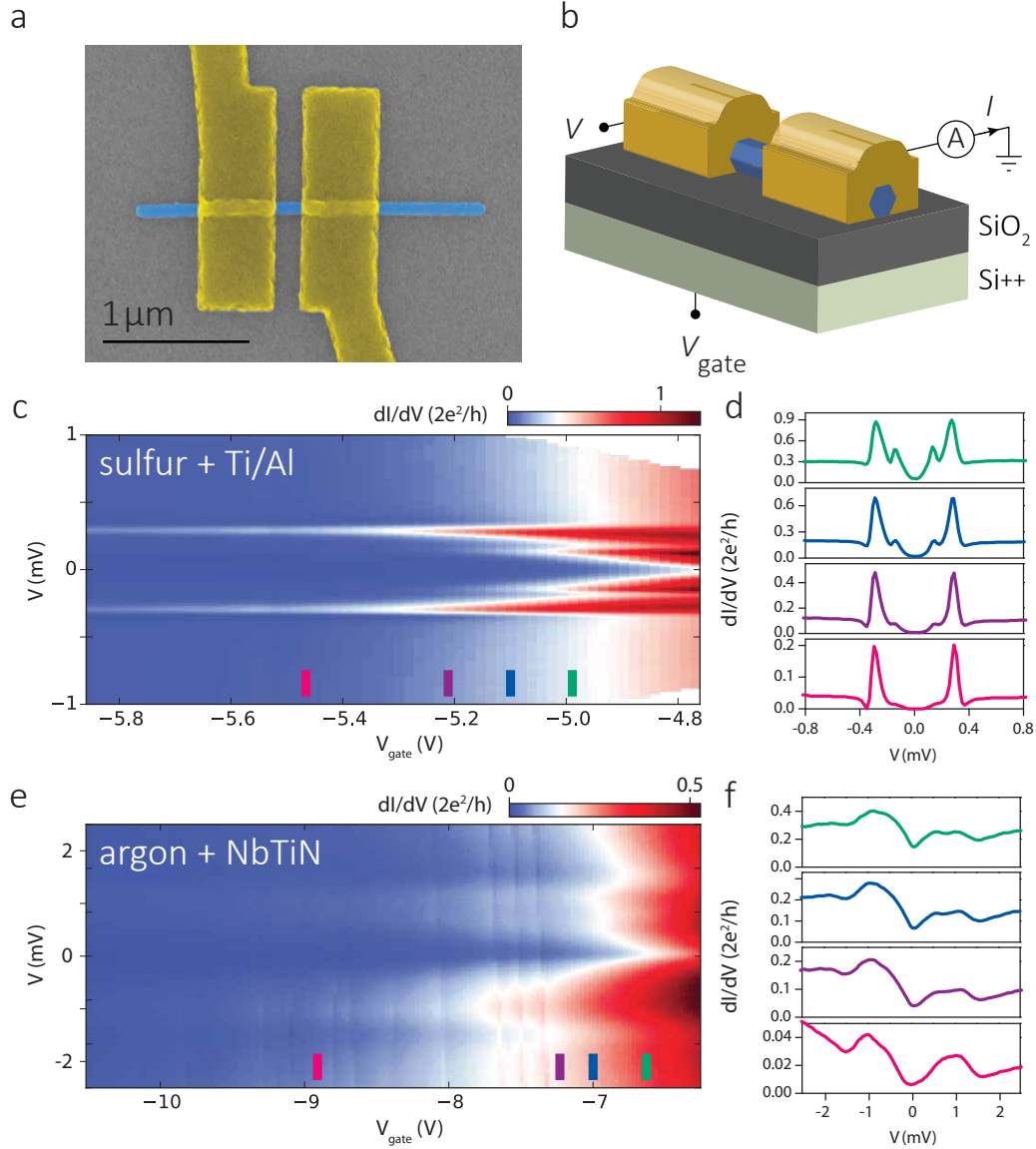


Figure 1: InSb nanowire hybrid device and induced superconducting gaps for different device realizations. (a) Top-view false-color electron micrograph of a typical device consisting of an InSb nanowire (blue) with a diameter ~ 80 nm coupled to two superconducting electrodes (yellow) with ~ 150 nm separation. (b) Schematic of the devices and the measurement setup with bias voltage V , monitored current I , and the voltage V_{gate} applied on back gate (Si++ substrate) that is separated from the device by a 285 nm thick SiO_2 dielectric. (c), (d) Spectroscopy of a device realized using sulfur cleaning followed by evaporation of superconducting Ti/Al (5/130 nm) electrodes. $T = 250$ mK. Differential conductance dI/dV is plotted as a function of bias voltage V for varying gate voltages V_{gate} . dI/dV traces in (d) are vertical line cuts from (c) at gate voltages marked with colored bars. dI/dV is symmetric around zero bias with two conductance peaks at $V \sim \pm 0.3$ mV seen for all gate voltages that result from the coherence peaks in the superconducting density of states at the edge of the induced gap Δ . For our device geometry with two superconducting electrodes $2\Delta \sim 0.3$ meV. For sufficiently low V_{gate} , where $dI/dV \ll 2e^2/h$ at above-gap bias ($V > 2\Delta$), tunnelling is weak, which suppresses the Andreev reflection probability revealing a hard induced gap. Larger gate voltages decrease the tunnel barrier height where increased Andreev reflection probability results in finite subgap conductance. (e), (f) Spectroscopy of a device realized using argon cleaning followed by sputtering of superconducting NbTiN (90 nm) electrodes. $T = 250$ mK. We find $2\Delta \sim 1$ meV, much larger than that of the Al-based InSb hybrid device shown above. dI/dV traces in (f) show an above-gap conductance comparable to those in (d). The induced gap is soft with a nonvanishing subgap conductance even for the weak tunnelling regime at low V_{gate} , indicating a deviation from Andreev transport.

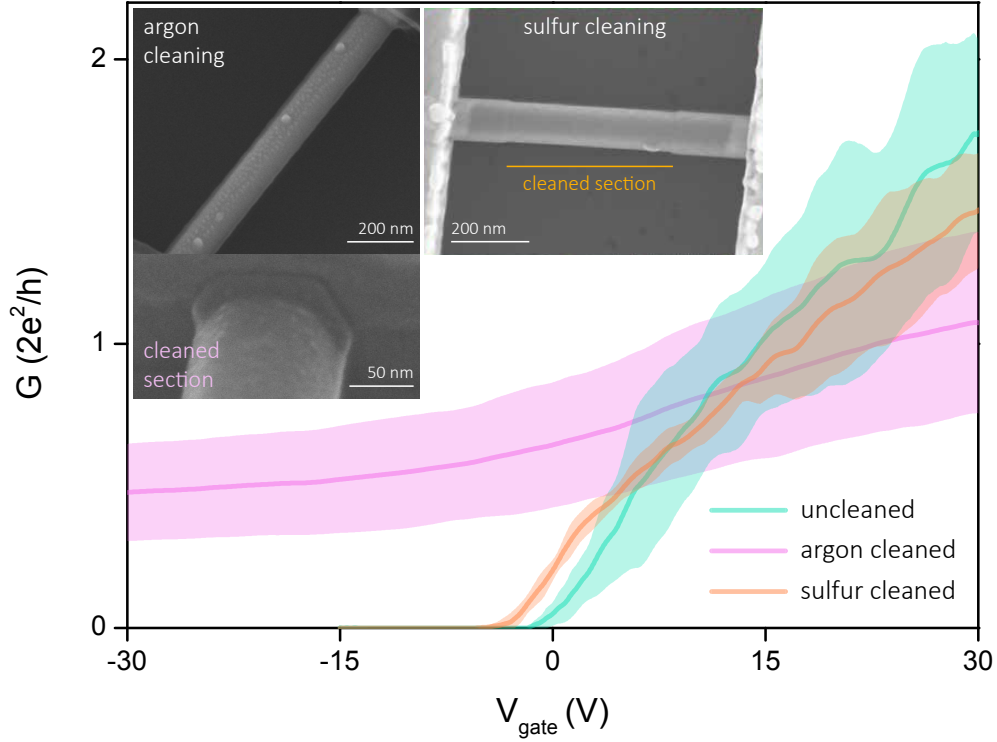


Figure 2: Effects of different surface cleaning on transport properties. Gate voltage dependent conductance G of InSb nanowire devices with $\sim 1 \mu\text{m}$ electrode separation (channel length) for argon-cleaned (pink), sulfur-cleaned (orange), and uncleaned pristine (cyan) channels. $T = 4 \text{ K}$. Traces represent ensemble-averaged conductance over 6 (argon-cleaned), 3 (sulfur-cleaned), and 2 (uncleaned) different devices measured at bias voltage $V = 10 \text{ mV}$, with the shades indicating the standard deviation (see Supporting Information for the details of averaging). Argon-cleaned channels do not pinch off, a deviation from a semiconducting gate response, and show a low transconductance $\propto dG/dV_{\text{gate}}$ indicating a low mobility. In contrast, sulfur-cleaned channels show a gate response similar to the pristine channel but with a shift of the threshold voltage towards negative values. Insets show high-resolution electron micrographs of argon- and sulfur-cleaned channels. Argon cleaning typically rounds the otherwise hexagonal cross section of the InSb nanowire (bottom image) and leaves a rough surface (top image). A sulfur cleaning yielding comparable contact resistances etches the InSb nanowire much less and leaves behind a smoother surface.

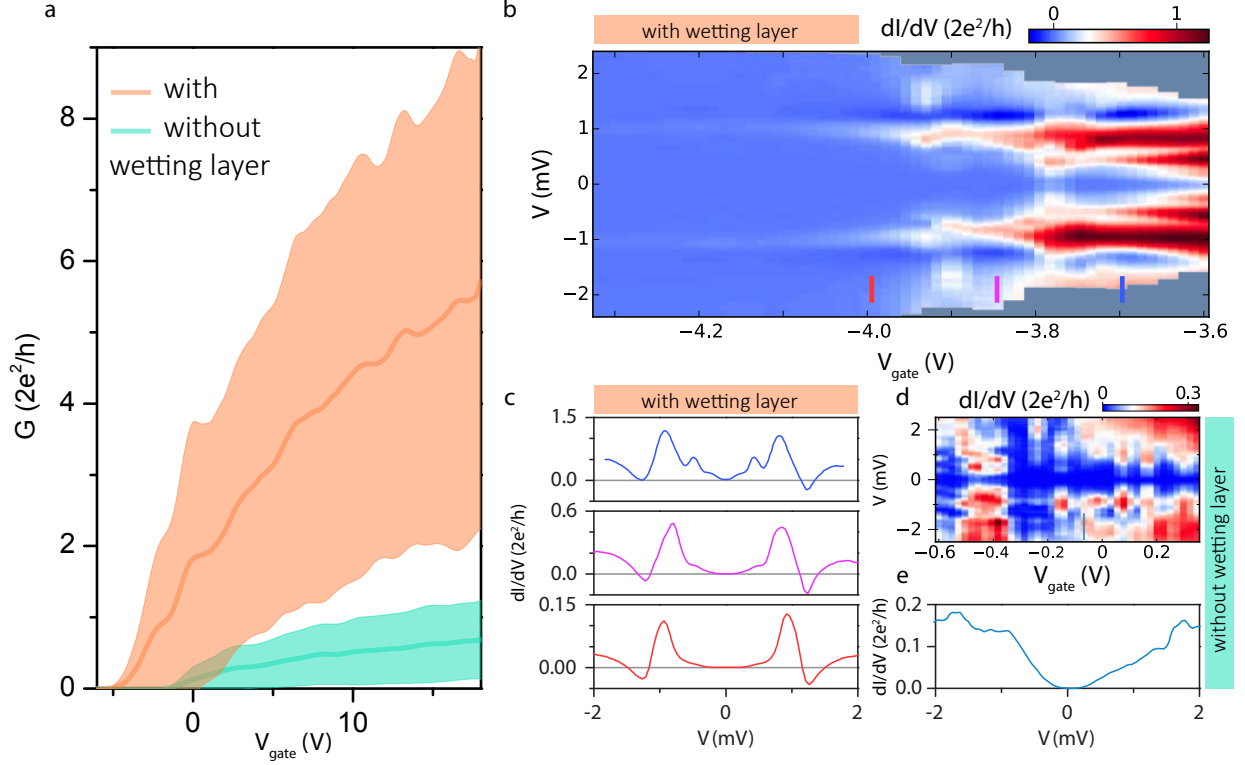


Figure 3: Effects of wetting layer on the transport and superconducting properties. (a) Gate voltage dependent conductance G of InSb nanowires devices with ~ 150 nm electrode separation realized with and without including a NbTi (5 nm) wetting layer between the nanowire and NbTiN (90 nm) electrodes. Native oxide on the nanowire surface is removed by sulfur cleaning prior to the deposition of the electrodes. Traces represent ensemble-averaged conductance over 4 (NbTi/NbTiN) and 7 (NbTiN) different devices measured at a bias voltage $V = 10$ mV, with the shades indicating the standard deviation (see Supporting Information for the details of averaging). Inclusion of a NbTi wetting layer decreases the average contact resistance (including both contacts) from ~ 100 k Ω to ~ 1.6 k Ω (see Supporting Information for the extraction of contact resistance). As a result, many quantized plateaus can be identified in ensemble-averaged conductance of NbTi/NbTiN devices (higher plateaus appear at slightly lower conductance due to the contact resistance). (b), (c) Spectroscopy of a device realized with NbTi/NbTiN electrodes. Differential conductance dI/dV is plotted as a function of bias voltage V for varying gate voltages V_{gate} . dI/dV traces in (c) are vertical line cuts from (b) at gate voltages marked with colored bars. dI/dV is symmetric in bias with two peaks at $V \sim \pm 1$ mV seen for all gate voltages from which we find $2\Delta \sim 1$ meV. For low V_{gate} and away from quantum dot resonances subgap conductance vanishes, revealing a hard induced gap. Larger gate voltages decrease the tunnel barrier height, where increased Andreev reflection probability results in finite subgap conductance. (d) Spectroscopy of a device realized with NbTiN electrodes without a NbTi wetting layer. Tunneling conductance is dominated by Coulomb blockade with irregular diamonds. Induced gap cannot be clearly identified. (e) A vertical line cut from (d) at $V_{\text{gate}} \sim -0.08$ V (indicated by a blue bar) with a conductance similar to the middle panel in (c). dI/dV is not symmetric in bias and coherence peaks are not visible. All data in this figure taken at $T = 250$ mK.

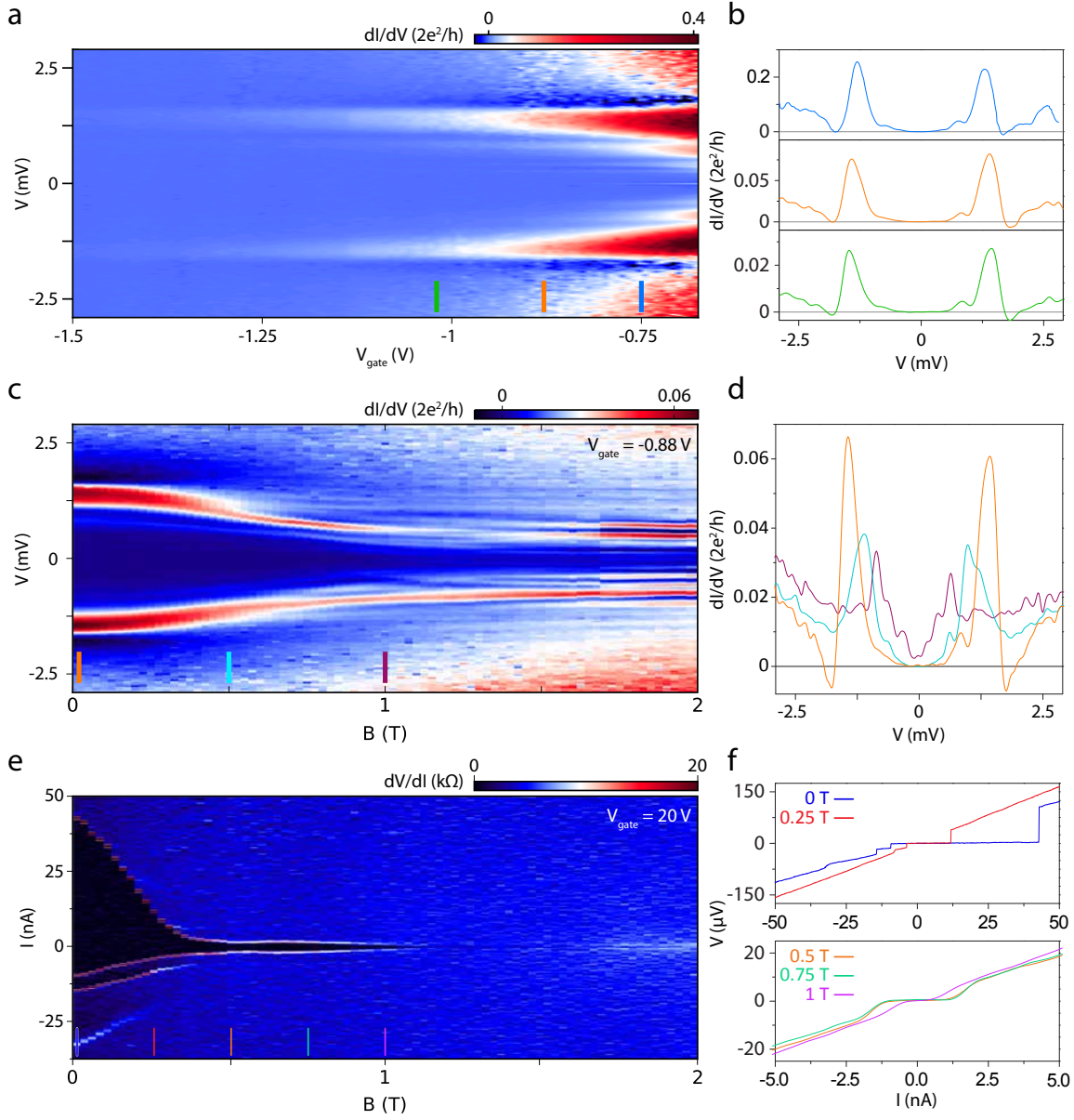


Figure 4: Tunneling spectroscopy and magnetic field response of InSb nanowire hybrid devices with engineered interface. (a), (b) Spectroscopy of a device realized with NbTi/NbTiN electrodes using sulfur cleaning followed by an *in-situ* low-power argon cleaning. Differential conductance dI/dV is plotted as a function of bias voltage V for varying gate voltages V_{gate} . dI/dV traces in (b) are vertical line cuts from (a) at gate voltages marked with colored bars. dI/dV is symmetric in bias with two peaks at $V \sim \pm 1.5$ mV seen for all gate voltages from which we find $2\Delta \sim 1.5$ meV. The induced gap is hard with vanishing subgap conductance in the tunneling regime. (c), (d) dI/dV of the same device is plotted as a function of bias voltage V for an increasing magnetic field B along the nanowire. Gate voltage is set to $V_{\text{gate}} = -0.88$ V, the same as in the middle panel in (b). dI/dV traces in (d) are vertical line cuts from (c) at magnetic fields marked with colored bars. The induced gap remains hard up to ~ 0.5 T. Increasing fields decrease the induced gap size and increase the subgap conductance but induced superconductivity persists up to 2 T where dI/dV shows a gap feature with suppressed conductance at small bias and symmetrically positioned coherence peaks. (e) Differential resistance dV/dI of an identical device is plotted as a function of bias current I for an increasing magnetic field B along the nanowire. Dark regions with vanishing resistance indicate the supercurrent which remains finite up to 1 T. Gate voltage $V_{\text{gate}} = 20$ V. (f) Current-voltage traces from (e) at magnetic fields marked with colored bars. We find a switching current of ~ 40 nA at zero magnetic field, which decreases to ~ 10 nA at 0.25 T, and to ~ 0.5 nA at 1 T. All data in this figure taken at $T = 50$ mK.

Supporting Information: Hard superconducting gap in InSb nanowires

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Author contributions. ÖG, FKdV, KZ, and VM developed the noninvasive surface cleaning and the inclusion of wetting layer. ÖG, HZ, and JvV optimized the noninvasive surface cleaning. SCB did the TEM analysis. MPN did the theoretical analysis. DJvW contributed to device fabrication. MQP and MCC optimized the NbTiN films. AG contributed to the data analysis. SK prepared the lamellae for TEM analysis. DC, SRP, and EPAMB grew the InSb nanowires. ÖG wrote the manuscript with contributions from all authors. LPK supervised the project.

List of supporting text and figures

Nanowire growth and device fabrication

Fabrication details of the long-channel devices in Fig 2

Measurement setup

Details of ensemble averaging

Extraction of contact resistance

Supporting Fig 1: Magnetic field response of the induced gap in InSb nanowire hybrid device with Ti/Al electrodes

Supporting Fig 2: Cross-sectional transmission electron micrographs of the nanowire surface cleaned using different methods

Supporting Fig 3: Additional transport properties of InSb nanowire hybrid devices with Ti/Al electrodes

Supporting Fig 4: Supercurrent in InSb nanowire hybrid devices with NbTi/NbTiN electrodes

Supporting Fig 5: Supercurrent in InSb nanowire hybrid devices with NbTi/NbTiN electrodes at $T = 50$ mK

Supporting Fig 6: Additional transport properties of InSb nanowire hybrid device with engineered interface (device A)

Supporting Fig 7: Additional transport properties of InSb nanowire hybrid device with engineered interface (device B)

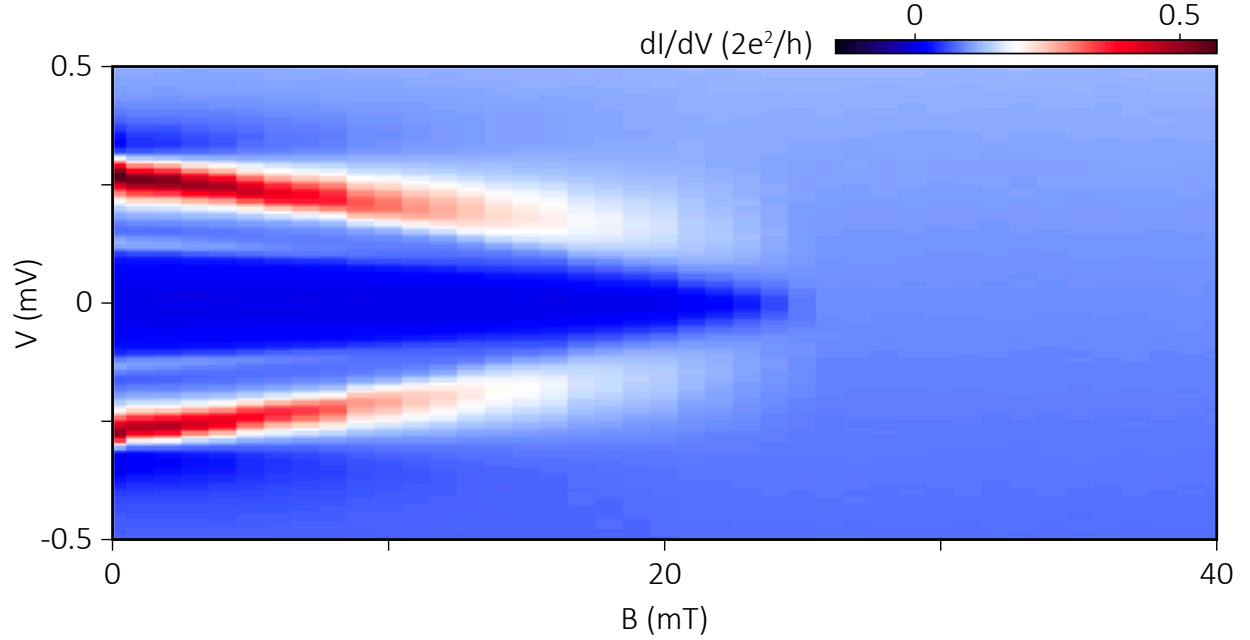
Nanowire growth and device fabrication. InSb nanowires have been grown by Au-catalyzed Vapor-Liquid-Solid mechanism in a Metal Organic Vapor Phase Epitaxy reactor. The InSb nanowire crystal direction is [111] zinc blende, free of stacking faults and dislocations.¹ Nanowires are deposited one-by-one using a micro-manipulator² on a p-Si++ substrate covered with 285 nm thick SiO₂ serving as a dielectric for back gate. Superconductor deposition process starts with resist development followed by oxygen plasma cleaning. For sulfur cleaning, the chip is immersed in a Sulfur-rich ammonium sulfide solution diluted by water (with a ratio of 1:200) at 60°C for half an hour.³ At all stages care is taken to expose the solution to air as little as possible. Ti/Al contacts are e-beam evaporated at a base pressure $< 10^{-7}$ mbar. In-situ argon plasma cleaning and NbTiN deposition is performed in an AJA International ATC 1800 sputtering system with a base pressure $\sim 10^9$ Torr. For devices without sulfur cleaning, argon cleaning is performed using an argon plasma typically at a pressure of 3 mTorr and a power of 100 Watts applied for 150 seconds, but different plasma parameters removing a similar thickness of InSb from the nanowire surface (> 15 nm) gave similar transport properties. For devices with sulfur cleaning we used a much milder argon plasma at a pressure of 10 mTorr and a power of 25 Watts applied for ~ 5 seconds. For NbTiN deposition a Nb_{0.7}Ti_{0.3} wt. % target with a diameter of 3 inches is used. Reactive sputtering resulting in (NbTi) NbTiN films was performed in an Ar/N process gas with (0) 8.3 at. % nitrogen content at a pressure of 2.5 mTorr using a dc magnetron sputter source at a power of 250 Watts. An independent characterization of the NbTiN films gave a critical temperature of 13.5 K for 90 nm thick films with a resistivity of $114 \mu\Omega\cdot\text{cm}$ and a compressive stress on Si substrate.

Fabrication details of the long-channel devices in Fig 2. For the InSb nanowire devices with sulfur-cleaned channels, the cleaning of the channel is performed after a complete fabrication of the electrodes contacting the nanowire. For the devices whose transport data is presented, sulfur cleaning is applied to the entire channel, while the inset shows a partially cleaned channel to illustrate the mild etching of the wire. For the nanowire devices with argon-cleaned channels, the cleaning of the channel is performed before the fabrication of the contact electrodes. However, we obtained a similar result when argon cleaning was applied after fabricating the contacts. For all long-channel devices we used argon cleaning to remove the native oxide on the nanowire surface prior to contact deposition.

Measurement setup. All the data in this study is measured using RC, copper powder, and π filters thermalized at different temperatures. Differential conductance measurements are performed using standard ac lock-in techniques. Nanowire devices are kept in vacuum during low temperature measurements.

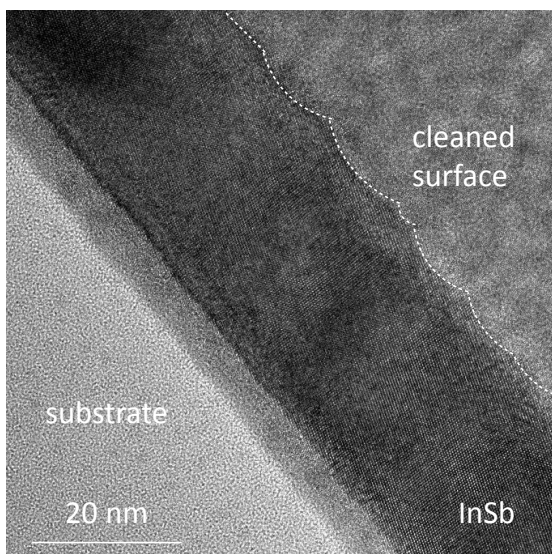
Details of ensemble averaging. Conductance is averaged over different nanowire devices for each value of gate voltage. Devices within an ensemble are fabricated simultaneously on a single substrate, have identical geometries, and are measured during the same cool down.

Extraction of contact resistance. We extract contact resistances by fitting the conductance measured as a function of gate voltage using the method described in S.Ref. 4. Here we leave the product of capacitance and mobility as a free fit parameter which is not taken into consideration.

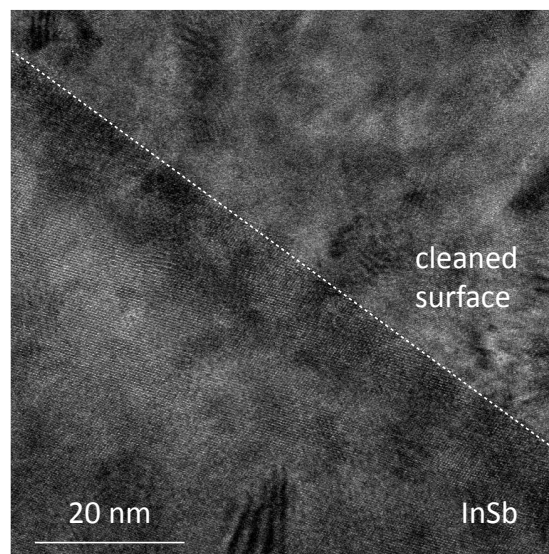


Supporting Figure 1: **Magnetic field response of the induced gap in InSb nanowire hybrid device with Ti/Al electrodes.** Differential conductance dI/dV is plotted as a function of bias voltage V for increasing magnetic field B along the nanowire axis. The nanowire device is in the tunneling regime with $dI/dV \ll 2e^2/h$ for above-gap bias ($V > 2\Delta$). At zero magnetic field dI/dV shows two conductance peaks at $V \sim \pm 0.3$ mV symmetric around zero bias giving $2\Delta \sim 0.3$ meV. Increasing the magnetic field decreases the size of the superconducting gap Δ which completely vanishes at ~ 25 mT. The device shows no superconductivity at larger magnetic fields. Device realized by sulfur cleaning. Ti/Al electrodes have a thickness of 5/130 nm and a separation of ~ 150 nm on the nanowire. $T = 50$ mK.

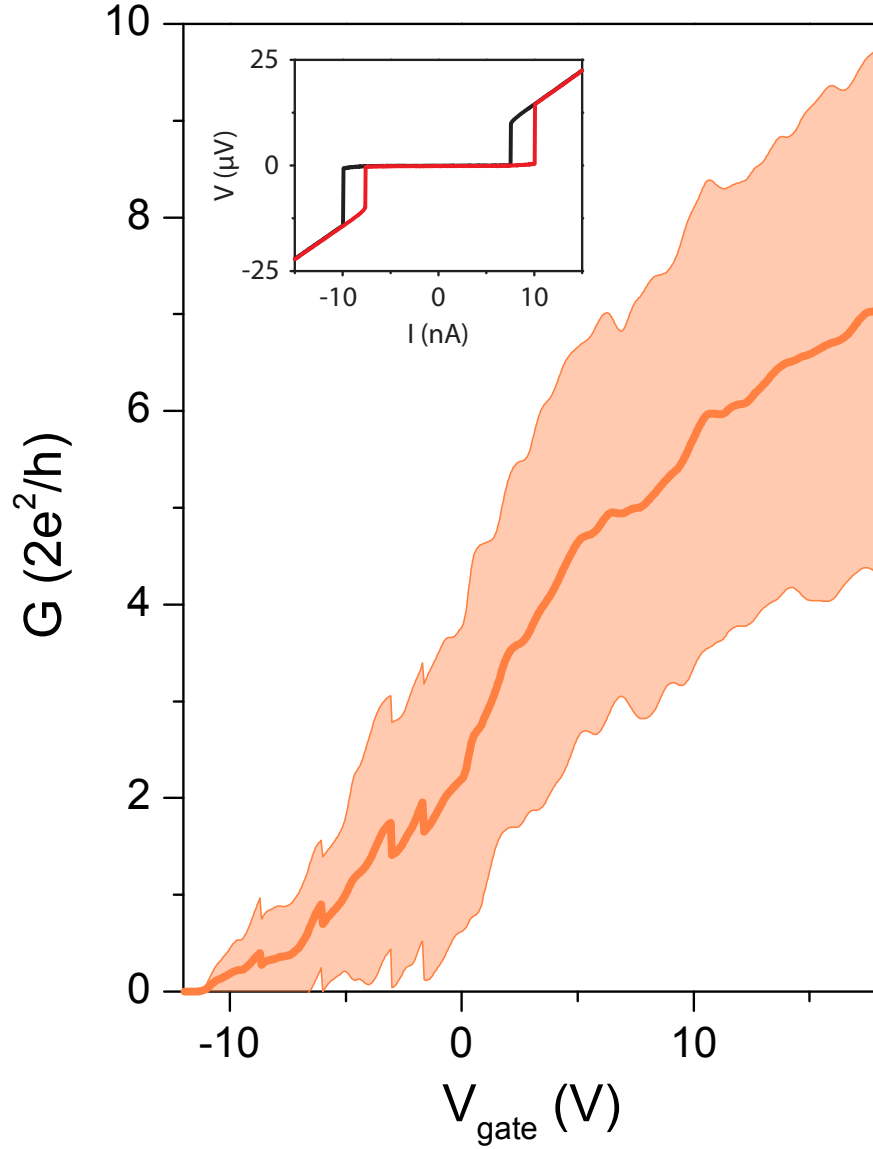
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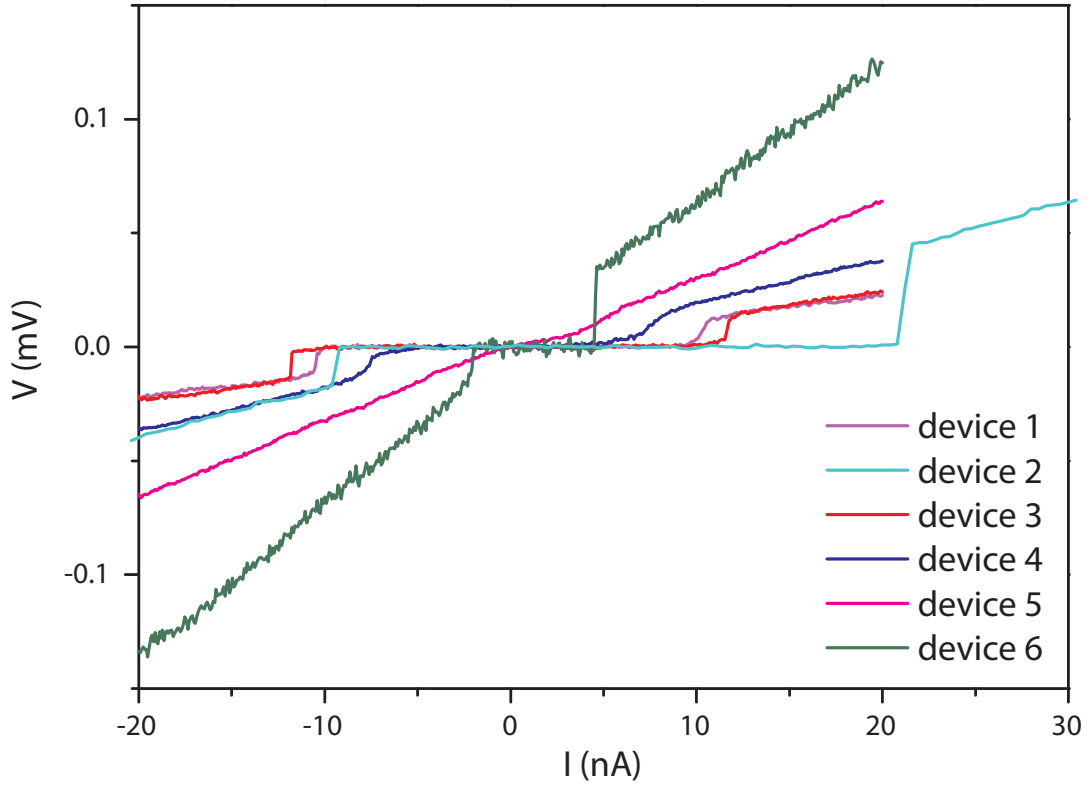
(b)



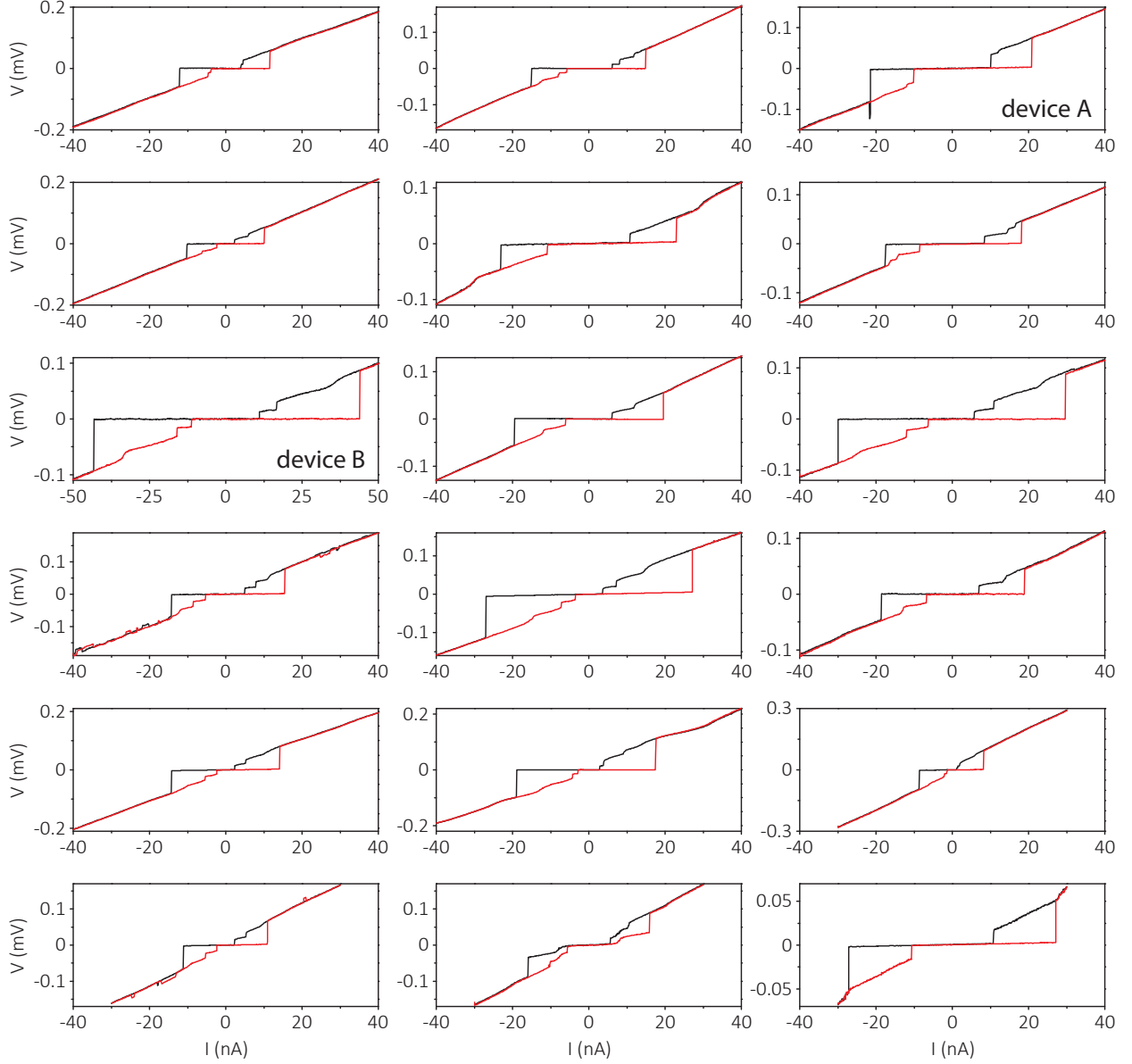
Supporting Figure 2: **Cross-sectional transmission electron micrographs of the nanowire surface cleaned using different methods.** The cuts were performed along the nanowire axis. **(a)** InSb nanowire surface after argon plasma cleaning. Argon cleaning leaves a rough nanowire surface. Nanowire appears thinner due to substantial etching. **(b)** InSb nanowire surface after sulfur cleaning followed by a low-power argon cleaning (see main text for details). Sulfur cleaning leaves a smoother nanowire surface.



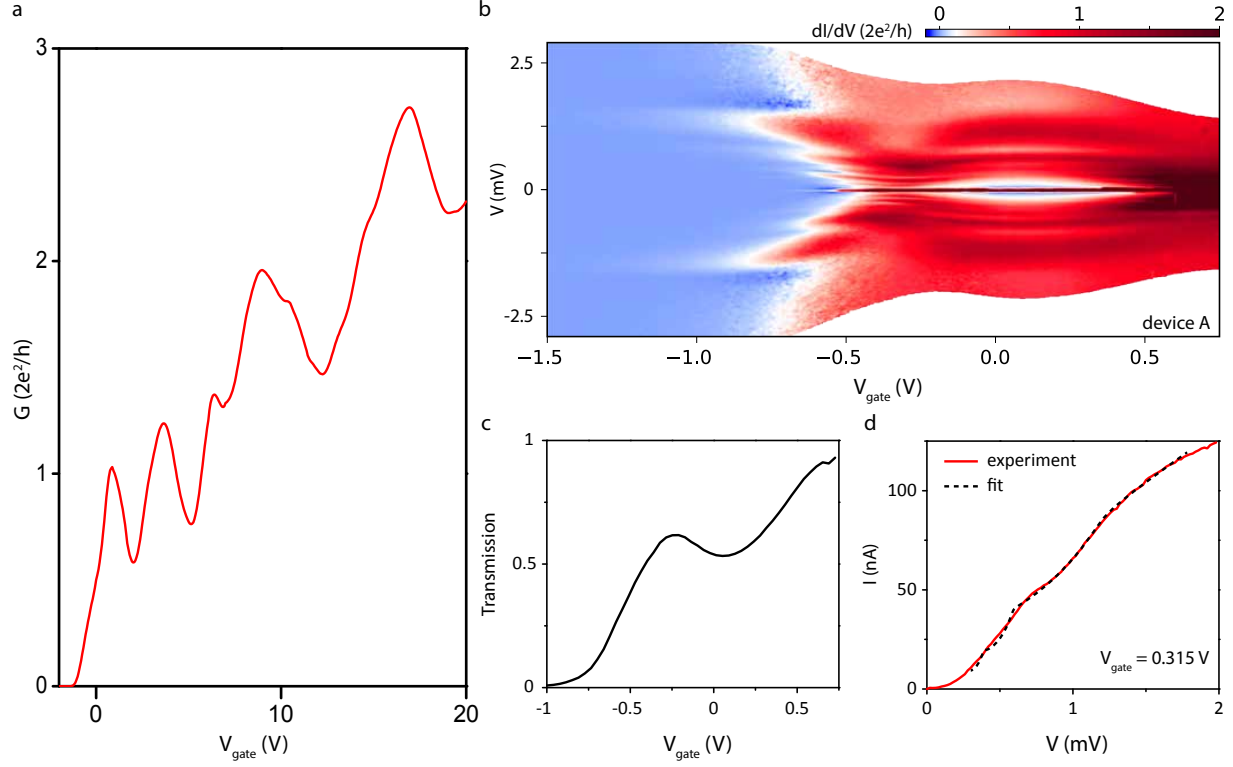
Supporting Figure 3: **Additional transport properties of InSb nanowire hybrid devices with Ti/Al electrodes.** Conductance G of InSb nanowire devices is plotted as a function of gate voltage V_{gate} . The trace represents ensemble-averaged conductance over 6 different devices on a single chip and the shade indicates the standard deviation. Taken at a bias voltage $V = 10$ mV. Average contact resistance (including both contacts) is ~ 1 k Ω . Inset shows voltage drop V as a function of bias current I for one of the 6 devices. We find a clear supercurrent up to ~ 10 nA. Red trace shows the current-voltage response when the bias current is swept in positive direction, black trace the negative direction. Gate voltage is set to $V_{\text{gate}} = 9$ V. Ti/Al electrodes have a thickness of 5/130 nm and a separation of ~ 150 nm on the nanowire. All data in this figure taken at $T = 250$ mK.



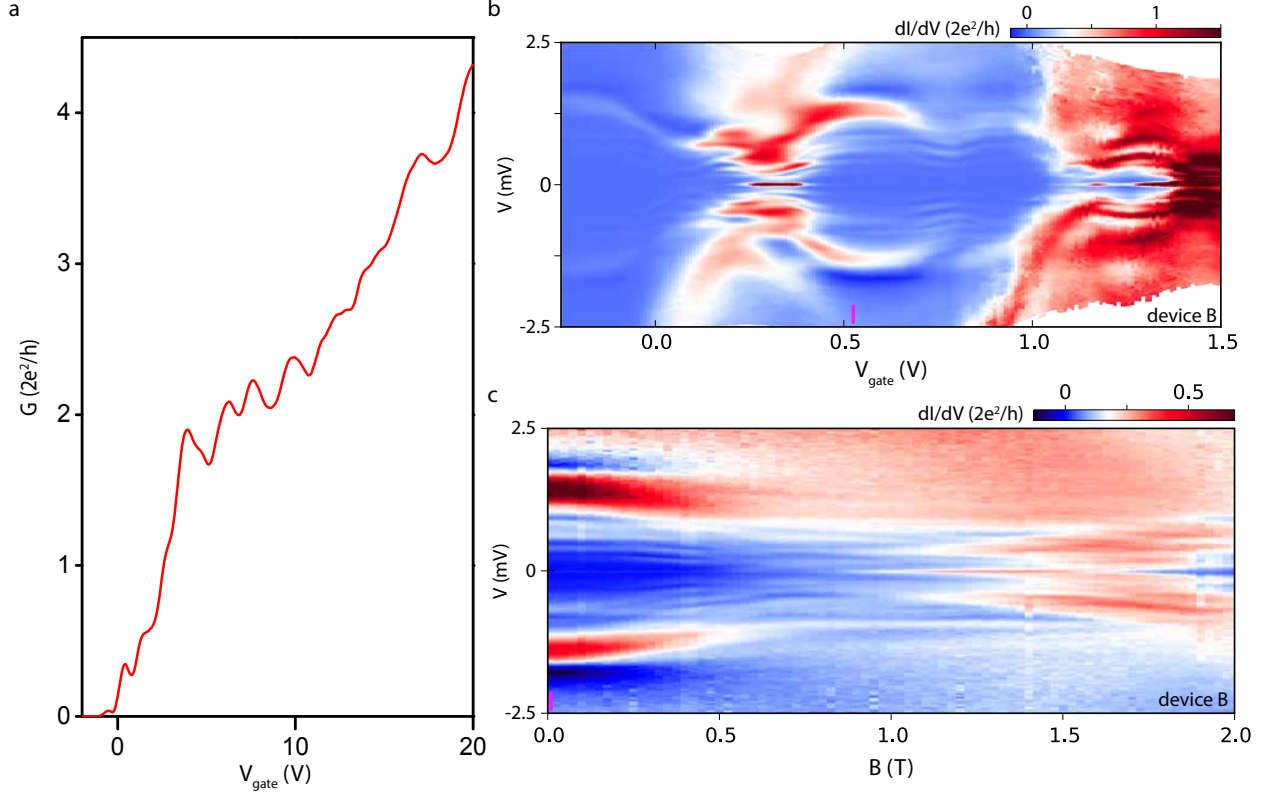
Supporting Figure 4: **Supercurrent in InSb nanowire hybrid devices with NbTi/NbTiN electrodes.** Devices realized using sulfur cleaning followed by an *in-situ* low-power argon cleaning. $T = 250$ mK. Voltage drop V is plotted as a function of bias current I for different devices on a single chip with 8 devices in total. An *in-situ* low-power argon cleaning improves the small bias response allowing to resolve a supercurrent for a high yield of devices. Gate voltage is set to $V_{\text{gate}} = 18$ V. NbTi/NbTiN electrodes have a thickness of 5/90 nm and a separation of ~ 150 nm on the nanowire.



Supporting Figure 5: Supercurrent in InSb nanowire hybrid devices with NbTi/NbTiN electrodes at $T = 50$ mK. Devices realized using sulfur cleaning followed by an *in-situ* low-power argon cleaning. Voltage drop V is plotted as a function of bias current I for all devices on a single chip. We find a clear supercurrent in every device. Red traces show the current-voltage response when the bias current is swept in positive direction, black traces the negative direction. We relate the origin of the hysteresis to electron heating.⁵ Gate voltage is set to $V_{\text{gate}} = 20$ V. NbTi/NbTiN electrodes have a thickness of 5/90 nm and a separation of ~ 150 nm on the nanowire. Data in main text Fig 4a-d is taken from Device A, data in main text Fig 4e,f taken from Device B.



Supporting Figure 6: **Additional transport properties of InSb nanowire hybrid device with engineered interface (device A).** All data in this figure is taken from device A, the device in main text Fig 4a-d. **(a)** Conductance G of InSb nanowire device is plotted as a function of gate voltage V_{gate} , taken at a bias voltage $V = 10$ mV. Extracted contact resistance (including both contacts) ~ 1.6 k Ω . **(b)** Differential conductance dI/dV is plotted as a function of bias voltage V for a large gate voltage V_{gate} range. **(c)** Transmission T extracted from (b) by fitting the measured current I using Averin-Bardas model.^{6,7} Best fit is obtained for a single channel transport through the nanowire. Transmission reaches ~ 0.9 giving a lower bound on contact transparency assuming a single channel transport. We note that our model does not account for the observed finite contact transparencies and conductance resonances, decreasing the certainty of our estimate. **(d)** The measured current I and the corresponding fit is plotted for $V_{\text{gate}} = 0.315$ V.



Supporting Figure 7: **Additional transport properties of InSb nanowire hybrid device with engineered interface (device B).** All data in this figure is taken from device B, the device in main text Fig 4e,f. **(a)** Conductance G of InSb nanowire device is plotted as a function of gate voltage V_{gate} , taken at a bias voltage $V = 10$ mV. Extracted contact resistance (including both contacts) ~ 1.2 k Ω . **(b)** Differential conductance dI/dV is plotted as a function of bias voltage V for varying gate voltages V_{gate} . Differential conductance shows quantum dot features similar to those previously reported for InSb nanowires.⁸ Further, we find subgap conductance peaks running through consecutive Coulomb valleys which we attribute to Andreev bound states in the wire section underneath the superconducting electrodes.⁹ For our device geometry with a back gate controlling both the conductance in the wire section between the electrodes as well as the occupation in the wire section underneath the electrodes, it is not possible to tune the device away from the subgap states while maintaining the tunnelling regime necessary for spectroscopy. **(c)** Differential conductance dI/dV is plotted as a function of bias voltage V for an increasing magnetic field B along the nanowire. $V_{\text{gate}} \sim 0.5$ V indicated with a pink bar in (b). Increasing magnetic fields bring the subgap states to lower energies resulting in a finite subgap conductance for $B > 0.3$ Tesla, similar to a previous report⁹ but at a relatively lower magnetic field.

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