LETTER

Epitaxy of advanced nanowire quantum devices

Sasa Gazibegovic[1,2]*, Diana Car[1,2]*, Hao Zhang[1]*, Stijn C. Balk[1], John A. Logan[3], Michiel W. A. de Moor[1], Maja C. Cassidy[1], Rudi Schmits[4], Di Xu[1], Guanzhong Wang[1], Peter Krogstrup[5], Roy L. M. Op het Veld[1,2], Kun Zuo[1], Yoram Vos[1], Jie Shen[1], Daniël Bouman[1], Borzoyeh Shojaei[3], Daniel Pennachio[3], Joon Sue Lee[6], Petrus J. van Veldhoven[2], Sebastian Koelling[2], Marcel A. Verheijen[2,7], Leo P. Kouwenhoven[1,8], Chris J. Palmstrøm[3,6,9] & Erik P. A. M. Bakkers[1,2]

Semiconductor nanowires are ideal for realizing various low-dimensional quantum devices. In particular, topological phases of matter hosting non-Abelian quasiparticles (such as anyons) can emerge when a semiconductor nanowire with strong spin–orbit coupling is brought into contact with a superconductor[1,2]. To exploit the potential of non-Abelian anyons—which are key elements of topological quantum computing—fully, they need to be exchanged in a well-controlled braiding operation[3–8]. Essential hardware for braiding is a network of crystalline nanowires coupled to superconducting islands. Here we demonstrate a technique for generic bottom-up synthesis of complex quantum devices with a special focus on nanowire networks with a predefined number of superconducting islands. Structural analysis confirms the high crystalline quality of the nanowire junctions, as well as an epitaxial superconductor–semiconductor interface. Quantum transport measurements of nanowire 'hashtags' reveal Aharonov–Bohm and weak-antilocalization effects, indicating a phase-coherent system with strong spin–orbit coupling. In addition, a proximity-induced hard superconducting gap (with vanishing sub-gap conductance) is demonstrated in these hybrid superconductor–semiconductor nanowires, highlighting the successful materials development necessary for a first braiding experiment. Our approach opens up new avenues for the realization of epitaxial three-dimensional quantum architectures which have the potential to become key components of various quantum devices.

Majorana zero modes are predicted to emerge once a superconductor is coupled to a semiconductor nanowire with a strong spin–orbit
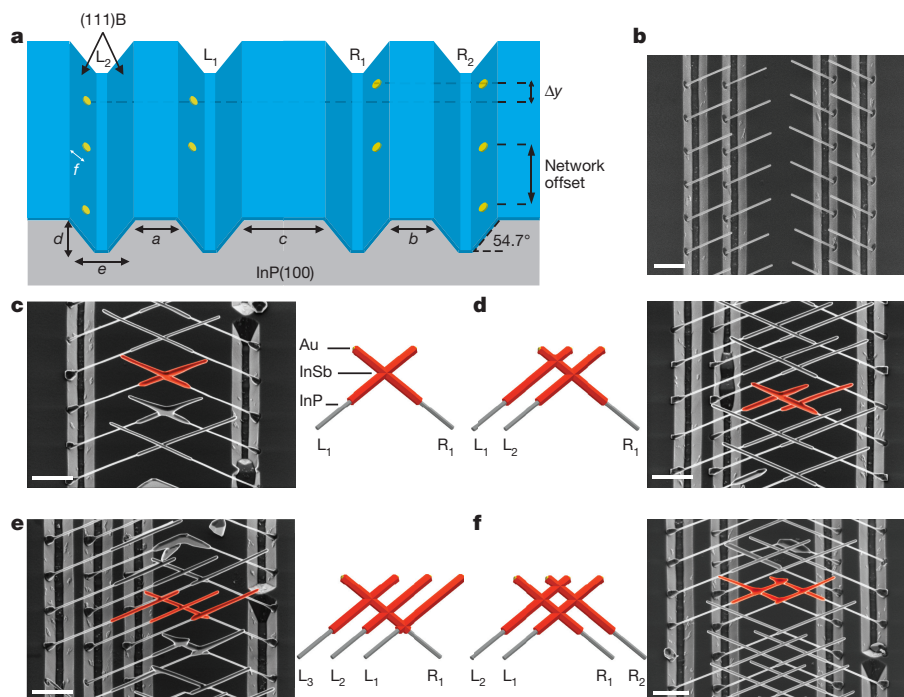

Figure 1 | Deterministic growth of InSb nanowire networks. a, Schematic illustration of the substrate with etched trenches. Gold catalysts are lithographically defined on the inclined facets. The offset between the catalyst particles (Δy) is critical for the realization of nanowire networks and shadowed superconducting islands. The size and the symmetry of the networks are controlled by the dimensions of the trenches indicated in the schematic: the spacing between the left–left (L_1, L_2), a, right–right (R_1, R_2), b, and left–right (L_1, R_1,) trenches, c, as well as the trench depth, d, width, e, and position of the gold particles on the inclined facets, f. **b**, A scanning electron microscopy (SEM) image of InP nanowires which serve as stems for InSb nanowire growth. **c–f**, SEM images and schematic illustrations of accomplished nanowire structures having one junction (**c**), two junctions (**d**), three junctions (**e**) or four junctions (**f**; hashtag). All SEM images are taken at 30° tilt. All scale bars are 1 μm.

[1]QuTech and Kavli Institute of NanoScience, Delft University of Technology, 2600 GA Delft, The Netherlands. [2]Department of Applied Physics, Eindhoven University of Technology, 5600 MB Eindhoven, The Netherlands. [3]Materials Department, University of California, Santa Barbara, California 93106, USA. [4]TNO Technical Sciences, Nano-Instrumentation Department, 2600 AD Delft, The Netherlands. [5]Center for Quantum Devices and Station-Q Copenhagen, Niels Bohr Institute, University of Copenhagen, 2100 Copenhagen, Denmark. [6]California NanoSystems Institute, University of California, Santa Barbara, California 93106, USA. [7]Philips Innovation Services Eindhoven, High Tech Campus 11, 5656 AE Eindhoven, The Netherlands. [8]Microsoft Station-Q at Delft University of Technology, 2600 GA Delft, The Netherlands. [9]Electrical and Computer Engineering, University of California, Santa Barbara, California 93106, USA.
*These authors contributed equally to this work.
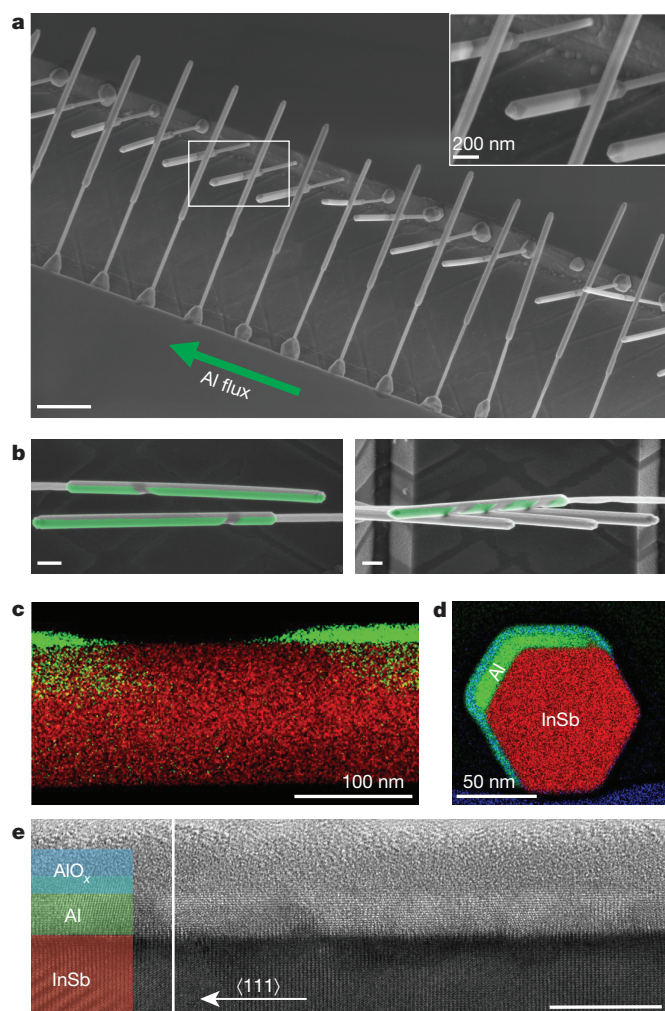
Figure 2 | Epitaxial growth of Al islands on InSb nanowires.
a, A 45°-tilted SEM image of an array of Al–InSb nanowires. The green arrow indicates the direction of Al beam flux during deposition. Scale bar is 1 μm. Inset, magnified area indicated by a white rectangle in the main panel. Each InSb nanowire is covered by two Al islands separated by a shadowed region. The number of shadows, n, and hence the number of superconducting islands, $n + 1$, is determined by the number of wires directly in front of the shadowed wire. **b**, SEM images of InSb nanowires with two (left) and four (right) Al islands (pseudo-coloured green). Both scale bars are 200 nm. **c**, STEM–EDX chemical composition map of an InSb nanowire (red) with Al islands (green) separated by an Al-free shadowed region. **d**, EDX chemical composition map of the nanowire cross-section. Al (green) is covering two out of the six {110} InSb side-facets. The Al–InSb interface is oxygen-free. **e**, High-resolution transmission electron microscopy image of an InSb nanowire (red) covered with a thin (about 10 nm), crystalline film of Al (green) and a layer of AlO_x (blue). InSb growth direction $\langle 111 \rangle$ is indicated by a white arrow. The image is taken along the $\langle 110 \rangle$ zone axis. The scale bar is 10 nm.

interaction in an external magnetic field[1,2]. InSb nanowires are a prime choice for this application owing to the large Landé g-factor (about 50) and strong Rashba spin–orbit interaction[9], crucial for the realization of Majorana zero modes. In addition, InSb nanowires generally show high mobility and ballistic transport[10–12]. Indeed, signatures of Majorana zero modes have been detected in hybrid superconductor–semiconductor InSb and InAs nanowire systems[11,13–15]. Multiple schemes for topological quantum computing based on braiding of Majorana zero modes have been reported, all employing hybrid nanowire networks[3–8].

Top-down fabrication of InSb nanowire networks is an attractive route towards scalability[16]; however, the large lattice mismatch between

InSb and insulating growth substrates limits the quality of the crystal. An alternative approach is bottom-up synthesis of out-of-plane nanowire networks which, owing to their large surface-to-volume ratio, effectively relieve strain on their sidewalls, enabling the growth of monocrystalline nanowires on highly lattice-mismatched substrates[17–19]. Recently, different schemes have been reported for merging nanowires into networks[20–22]. Unfortunately, these structures are either not monocrystalline, owing to a mismatch of the crystal structure of the wires with that of the substrate (that is, hexagonal nanowires on a cubic substrate)[22], or the yield is low owing to limited control over the multiple accessible growth directions (the yield decreases with the number of junctions in the network)[23].

Here, we develop a technique for bottom-up synthesis of monocrystalline InSb nanowire networks with an unprecedented yield of crossed junctions. Accurate control over the nanowire position and growth direction enables us to grow complicated networks of up to four crossed junctions, such as closed loops of four interconnected nanowires (referred to as 'hashtags'). Furthermore, this platform allows *in situ* growth of a predefined number of separated superconducting islands on the nanowires. This eliminates the need for metal etching during device fabrication. Therefore, the integration of semiconductors with metals (for example, niobium) is possible without an additional etching process. This guarantees that the pristine atomically flat InSb(110) facets are left intact, a key element for high device performance. At the same time a clean epitaxial superconductor–nanowire interface is established, which has recently been proven to be crucial for the quality of the induced superconducting gap[24,25].

For the growth of the nanowire networks a substrate with trenches is first fabricated (see Fig. 1a). These structures are defined by electron-beam lithography, a reactive ion etch and a subsequent wet etch to expose (111)B facets on an InP(100) crystal surface (Fig. 1a). See Methods and Extended Data Fig. 1 for the fabrication of InP substrate with trenches. A second lithography step is then used to position gold particles, which catalyse nanowire growth via the vapour–liquid–solid mechanism, on the inclined facets (Extended Data Figs 2 and 3). Owing to the geometry of the (111)B facets, the nanowires are forced to grow towards each other and can fuse into a network. The final size and symmetry of the networks are controlled by the dimensions of the trenches and the spacing between them, that is, the parameters a–f, as indicated in Fig. 1a and Extended Data Fig. 4. The left (right) trenches and wires grown from them are labelled L_1, L_2 (R_1, R_2). The offset (Δy) between the gold particles is an important parameter to control for two reasons. First, if $\Delta y < D$, where D is the nanowire diameter, nanowires will merge during growth (specifically, for $\Delta y \approx 0$ ($\Delta y \leq D$), resulting in the formation of a T-junction (X-junction)[23]; second, $\Delta y > D$ enables shadow growth of the superconducting islands, as discussed later in the text. In Fig. 1b we show a uniform array of InP nanowires that are used as stems to facilitate uniform nucleation of InSb nanowires. When InSb nanowires (highlighted in red in Fig. 1c–f) are grown on top of these InP stems, nanowire networks with 1–4 wire–wire junctions are formed, depending on the trench design (Fig. 1c–f). Importantly, this approach is generic and can be used to synthesize interconnected nanowires of various semiconductor materials which grow along a $\langle 111 \rangle$B direction. The number of wire–wire junctions can be increased by allowing for longer nanowire growth times and/or fabricating a larger number of left and right trenches. The high crystal quality of the InSb nanowire junctions is confirmed by high-resolution transmission electron microscopy (HRTEM) imaging of a hashtag structure (see Extended Data Fig. 5).

Next, we combine the nanowire-network geometry with the directionality of molecular beam epitaxy (MBE) to shadow-grow aluminium superconducting islands on the InSb wires. The aluminium flux is aligned parallel to the trenches (Fig. 2a), such that a frontal wire casts a shadow on a wire in the background (inset of Fig. 2a). This causes interruptions in a uniform layer of aluminium as shown in Fig. 2b (left). For effective shadowing, it is important that the frontal wire does not merge
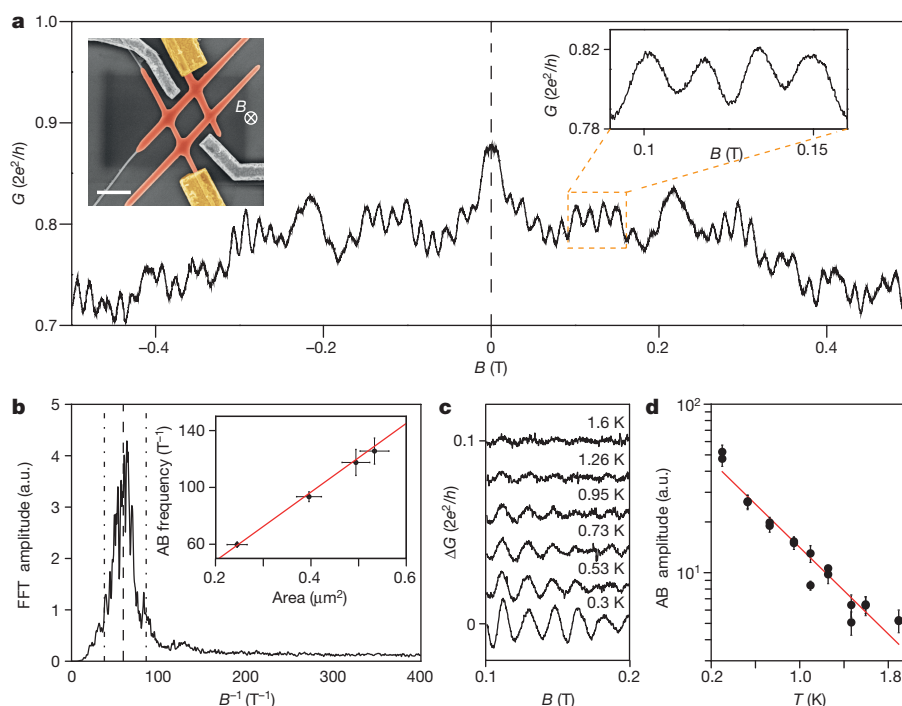
Figure 3 | Aharonov–Bohm and weak-antilocalization effects in nanowire hashtags. a, Magnetoconductance of a hashtag shows periodic Aharonov–Bohm oscillations and a weak-antilocalization peak at $B = 0$ T. Inset (left), a pseudo-coloured SEM image of the device. An InSb hashtag (red) is in contact with normal metal electrodes (yellow) and measured in an out-of-plane magnetic field at 300 mK. Scale bar is 500 nm. Inset (right), magnification of the region indicated by an orange rectangle in the main panel, containing four Aharonov–Bohm periods. **b**, FFT spectrum of the magnetoconductance of this device (ensemble averaged), indicating the Aharonov–Bohm (AB) oscillation frequency. The dashed line indicates the expected frequency based on the area calculated from the SEM image, dash-dotted lines indicate the expected minimum and maximum frequencies due to the finite thickness of the interferometer arms. Inset, plot of the peak frequency, assigned from the averaged FFT spectra, as a function of the loop area for four different hashtag devices. The red line corresponds to the expected frequency of an h/e periodic oscillation for a given loop area. a.u., arbitrary units. **c**, Temperature dependence of Aharonov–Bohm oscillations (background subtracted). The Aharonov–Bohm effect persists up to 1.6 K. Curves are offset vertically for clarity. **d**, Aharonov–Bohm (AB) amplitude as a function of temperature. The red line is a fit to the data, showing an exponential decay of the oscillation amplitude.

with the shadowed wire, that is, $\Delta y > D$. The number of shadows, n, (and, accordingly, the number of superconducting islands, $n + 1$) on any InSb nanowire is determined by the number of wires directly in front of that nanowire. For example, Fig. 2b (right) and Extended Data Fig. 6 depict an InSb nanowire with three shadows cast by three frontal nanowires. The position and the width of the shadows are uniform for all wires examined and are set by the relative position of the wires and the solid angle of the aluminium effusion cell. The abrupt transition between the shadowed region of the nanowire and the segment covered with aluminium is evident from the chemical composition map (Fig. 2c) acquired by energy-dispersive X-ray spectroscopy (EDX) combined with scanning transmission electron microscopy (STEM). The line-of-sight directionality of MBE growth results in aluminium being deposited on two out of six facets of an InSb nanowire, as can be seen from a STEM–EDX map of a nanowire cross-section (Fig. 2d). The partial coverage of a nanowire with aluminium is essential as it allows tuning of the electron density of the proximitized nanowire by an external gate electrode, which is necessary for accessing the topological phase. The epitaxial interface between the InSb nanowire and a uniform, thin layer of aluminium is revealed by HRTEM imaging (Fig. 2e). In the next section, we assess the electronic quality of our structures.

Phase-coherent transport is a basic requirement for certain measurement-based braiding schemes which make use of an interferometric readout[7,8]. This interferometer requires tuning towards a maximum amplitude of the Aharonov–Bohm oscillations. To investigate the Aharonov–Bohm effect in our nanowire networks, nanowire hashtags were transferred onto a SiO_2/p-Si substrate and contacted by metal electrodes (Au/Cr, Fig. 3a left inset). Figure 3a shows the

magnetoconductance of a representative device (device A). Periodic Aharonov–Bohm oscillations can clearly be seen (Fig. 3a right inset), as well as a pronounced weak-antilocalization conductance peak at $B = 0$ T. The weak-antilocalization conductance peak is present in most of the measured hashtag devices, for both in- and out-of-plane magnetic field orientations (Extended Data Fig. 7), indicating a strong spin–orbit coupling in this system. The observed weak-antilocalization effect also suggests diffusive transport in our hashtag devices, since the hashtag length is several times longer than the estimated mean free path, approximately 250 nm for InSb nanowires[10,26]. The period of the Aharonov–Bohm oscillations is extracted from a discrete Fourier transform of the magnetoconductance. Figure 3b shows the averaged fast Fourier transform (FFT) spectrum of which the peak frequency (60 T^{-1} with a standard deviation of 2 T^{-1}) corresponds to a period ΔB of 16.7 mT with a standard deviation of 0.6 mT. The effective area (A) calculated from this Aharonov–Bohm period ($A = \Phi/\Delta B = 0.25\,\mu m^2$ with a standard deviation of $0.01\,\mu m^2$, where $\Phi = h/e$ is the flux quantum) is in agreement with the measured area of a hashtag loop ($A \approx 0.25\,\mu m^2$ with a standard deviation of $0.02\,\mu m^2$). We determine the peak frequency for four different devices with different loop areas, showing good agreement with the expected values (Fig. 3b inset). This agreement between theory and experiment confirms that the observed Aharonov–Bohm oscillations are indeed a result of the quantum interference of electron waves emanating from the two transport channels that constitute the hashtag.

Magnetoconductance traces taken at increasing temperature values are shown in Fig. 3c. Aharonov–Bohm oscillations persist up to about 1.6 K. The amplitude of the Aharonov–Bohm oscillations decays
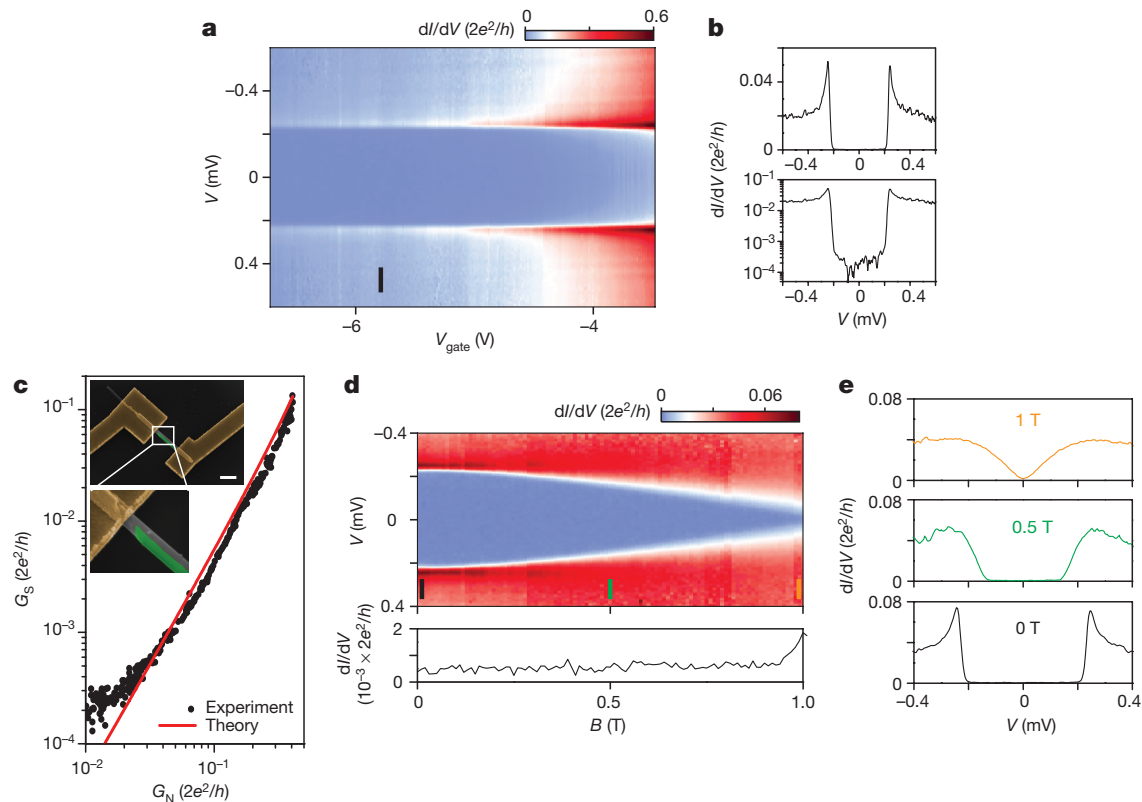
Figure 4 | Induced hard superconducting gap in a shadowed Al–InSb nanowire device. a, Differential conductance (dI/dV) as a function of bias voltage (V) and back gate voltage (V_{gate}) in the tunnelling regime, resolving a hard superconducting gap (at about 20 mK). **b**, A line cut taken at the position indicated by the black bar in **a** (at $V_{gate} = -5.8$ V), plotted on linear (left) and logarithmic scale (right). The ratio of above-gap and sub-gap conductance (G_N/G_S) reaches about 100. The induced superconducting gap size is $\Delta \approx 0.24$ meV. **c**, Sub-gap conductance as a function of above-gap conductance. The red line is the theoretical curve calculated assuming only Andreev processes[28]. Inset, a pseudo-coloured SEM image of the similar device. The device is an N (yellow)–nanowire (grey)–S (green) system. The scale bar is 500 nm. **d**, Magnetic field dependence of the superconducting gap ($V_{gate} \approx -5.7$ V) in the device. The magnetic field direction is aligned with the nanowire axis. The lower panel shows a horizontal line-cut taken at $V = 0$ V (in the middle of the superconducting gap). **e**, Vertical line cuts taken at positions indicated by a black ($B = 0$ T), green ($B = 0.5$ T) and orange bar ($B = 1$ T) in the upper panel in **d**, illustrating the evolution of the induced superconducting gap in the increasing magnetic field.

exponentially with temperature (Fig. 3d). This exponential behaviour, observed in early Aharonov–Bohm experiments with similar loop size[27], suggests that the phase coherence length is proportional to T^{-1}. Following the method described in ref. 27, we can estimate a phase coherence length on the basis of the suppression slope in Fig. 3d, to be 0.7 μm with a standard deviation of 0.1 μm at 1 K, which translates to 2.3 μm with a standard deviation of 0.3 μm at 300 mK.

The last essential requirement for a topological phase is induced superconductivity in the InSb nanowires. For this study, InSb wires with two superconducting islands were used to fabricate N–nanowire–S devices by replacing one superconducting island with a normal metal electrode (see Methods for the device fabrication recipe). The shadowed region of the nanowire is situated in between the normal contact and the other superconducting island, and can be depleted by a bottom gate (inset Fig. 4c), to form a tunnel barrier. In the tunnelling regime, the differential conductance reflects the quasiparticle density-of-states in the proximitized nanowire segment. Figure 4a shows a plot of differential conductance (dI/dV) versus bias voltage (V) and back-gate voltage (V_{gate}) at 20 mK. Hence, the two high-conductance horizontal lines (at $V = \pm 0.24$ mV) in Fig. 4a correspond to the superconducting coherence peaks. The shape of the superconducting gap can be clearly resolved in Fig. 4b, which shows a vertical line-cut plotted on both linear (left) and logarithmic (right) scales, indicating the ratio of the above-gap to sub-gap conductance $G_N/G_S \approx 100$. Figure 4c maps out the obtained values of G_S versus G_N (black dots) together with the Beenakker expression (red line) for an N–quantum point contact (QPC)–S system. This

expression assumes that G_S is due to a single-channel Andreev reflection in the shadowed region (see Extended Data Fig. 8)[28]. Theory and experiment are in agreement over two orders of magnitude in conductance. This shows that the G_S in this system is dominated by the Andreev process in the absence of quasiparticle transport. Figure 4d shows the differential conductance (dI/dV) of the same device as a function of bias voltage (V) and magnetic field (B) pointing along the nanowire, taken at $V_{gate} = -5.7$ V. From the horizontal line-cut at $V = 0$ V (lower panel), it can be seen that G_S is pinned to extremely low values of conductance for magnetic field values up to 0.9 T. The evolution of the induced superconducting gap in the magnetic field is illustrated in Fig. 4e. The black, green and orange line cuts are taken at $B = 0$ T, 0.5 T and 1 T, respectively. Importantly, the induced hard superconducting gap in Al–InSb nanowires endures up to $B \approx 0.9$ T, which surpasses the value of the magnetic field required for achieving a topological phase transition in InSb ($B \approx 0.2$ T)[1,2,11]. Extended Data Fig. 8 shows data of additional devices and the corresponding analysis.

The combination of phase-coherent transport in a network of nanowires and a hard superconducting gap in InSb nanowires, induced by local superconductor islands, is a substantial materials advancement that paves the road for the first Majorana braiding experiments. We emphasize that the platform developed in this work is generic and can be used for many different superconductor–semiconductor combinations, presenting opportunities in new quantum devices. For instance, devices working on the principle of beam splitting and interference of electrons (that is, Aharonov–Bohm interferometers, Cooper pair

splitters), as well as other, less-investigated quasiparticles, that is, phonons.

Online Content Methods, along with any additional Extended Data display items and Source Data, are available in the online version of the paper; references unique to these sections appear only in the online paper.

Received 8 April; accepted 23 June 2017.

1. Lutchyn, R. M. *et al.* Majorana fermions and a topological phase transition in semiconductor–superconductor heterostructures. *Phys. Rev. Lett.* **105,** 077001 (2010).
2. Oreg, Y. *et al.* Helical liquids and Majorana bound states in quantum wires. *Phys. Rev. Lett.* **105,** 177002 (2010).
3. Alicea, J. *et al.* Non-Abelian statistics and topological quantum information processing in 1D wire networks. *Nat. Phys.* **7,** 412–417 (2011).
4. Hyart, T. *et al.* Flux-controlled quantum computation with Majorana fermions. *Phys. Rev. B* **88,** 035121 (2013).
5. Aasen, D. *et al.* Milestones toward Majorana-based quantum computing. *Phys. Rev. X* **6,** 031016 (2016).
6. Plugge, S. *et al.* Majorana box qubits. *New J. Phys.* **19,** 012001 (2017).
7. Vijay, S. & Fu, L. Teleportation-based quantum information processing with Majorana zero modes. *Phys. Rev. B* **94,** 235446 (2016).
8. Karzig, T. *et al.* Scalable designs for quasiparticle-poisoning-protected topological quantum computation with Majorana zero modes. *Phys. Rev. B* **95,** 235305 (2017).
9. van Weperen, I. *et al.* Spin-orbit interaction in InSb nanowires. *Phys. Rev. B* **91,** 201413 (2015).
10. Kammhuber, J. *et al.* Conductance quantization at zero magnetic field in InSb nanowires. *Nano Lett.* **16,** 3482–3486 (2016).
11. Zhang, H. *et al.* Ballistic Majorana nanowire devices. Preprint at https://arxiv.org/abs/1603.04069 (2016).
12. Fadaly, E. M. T. *et al.* Observation of conductance quantization in InSb nanowire networks. *Nano Lett.* http://dx.doi.org/10.1021/acs.nanolett.7b00797 (2017).
13. Mourik, V. *et al.* Signatures of Majorana fermions in hybrid superconductor-semiconductor nanowire devices. *Science* **336,** 1003–1007 (2012).
14. Deng, M. T. *et al.* Majorana bound state in a coupled quantum-dot hybrid-nanowire system. *Science* **354,** 1557–1562 (2016).
15. Albrecht, S. M. *et al.* Exponential protection of zero modes in Majorana islands. *Nature* **531,** 206–209 (2016).
16. Shabani, J. *et al.* Two-dimensional epitaxial superconductor-semiconductor heterostructures: A platform for topological superconducting networks. *Phys. Rev. B* **93,** 155402 (2016).
17. Conesa-Boj, S. *et al.* Gold-free ternary III-V antimonide nanowire arrays on silicon: twin-free down to the first bilayer. *Nano Lett.* **14,** 326–332 (2014).
18. Plissard, S. R. *et al.* From InSb nanowires to nanocubes: looking for the sweet spot. *Nano Lett.* **12,** 1794–1798 (2012).
19. Caroff, P. *et al.* InSb heterostructure nanowires: MOVPE growth under extreme lattice mismatch. *Nanotechnology* **20,** 495606 (2009).
20. Dalacu, D. *et al.* Droplet dynamics in controlled InAs nanowire interconnections. *Nano Lett.* **13,** 2676–2681 (2013).
21. Kang, J.-H. *et al.* Crystal structure and transport in merged InAs nanowires MBE grown on (001) InAs. *Nano Lett.* **13,** 5190–5196 (2013).
22. Rieger, T. *et al.* Crystal phase transformation in self-assembled InAs nanowire junctions on patterned Si substrates. *Nano Lett.* **16,** 1933–1941 (2016).
23. Car, D. *et al.* Rationally designed single-crystalline nanowire networks. *Adv. Mater.* **26,** 4875–4879 (2014).
24. Krogstrup, P. *et al.* Epitaxy of semiconductor–superconductor nanowires. *Nat. Mater.* **14,** 400–406 (2015).
25. Gül, Ö. *et al.* Hard superconducting gap in InSb nanowires. *Nano Lett.* **17,** 2690–2696 (2017).
26. Gül, Ö. *et al.* Towards high mobility InSb nanowire devices. *Nanotechnology* **26,** 215202 (2015).
27. Hansen, A. E. *et al.* Mesoscopic decoherence in Aharonov–Bohm rings. *Phys. Rev. B* **64,** 045327 (2001).
28. Beenakker, C. W. J. Quantum transport in semiconductor–superconductor microjunctions. *Phys. Rev. B* **46,** 12841 (1992).

METHODS

Substrate fabrication. Fabrication of substrates with trenches is a three-step lithography process:

First, electron-beam lithography (EBL) and metal lift-off are used to deposit alignment markers on a (100) InP substrate.

Substrate cleaning. InP(100) wafer is cleaned with buffered oxide etch (NH_4F:HF = 7:1) (5 min), rinsed in H_2O, IPA (10 min)

Fabrication of markers. Spin resist AR-P 6200.13 at 6,000 r.p.m., bake at 150 °C for 3 min; write marker patterns using e-beam lithography (dose 300 μC cm^{-2}); developing in AR 600-546 for 1:30 min in ultrasonic agitation; ultrasonic rinse in IPA for 30 s, blow dry; evaporation of 80 nm Au; lift-off in PRS3000 at 88 °C for 2 h; rinse in warm (>50 °C) H_2O; rinse in IPA for 1 min, blow dry.

Second, the InP(100) wafer is cleaned in buffered oxide etch (NH_4F:HF = 7:1) for 5 min and exposed to O_2 microwave plasma to create a thin (about 2 nm) sacrificial layer of native oxide on the surface before deposition of 50 nm of SiO_x by plasma-enhanced chemical vapour deposition (PECVD). EBL and reactive ion etching (RIE) in CHF_3/Ar plasma are used to define rectangular openings in SiO_x, whose long edge is aligned with the [$0\bar{1}\bar{1}$] direction of the substrate. The alignment of the openings is crucial to achieve trenches with inclined (111)B facets after the subsequent anisotropic wet-etch step (HCl:H_3PO_4 = 5:1 (ref. 29), for 15 s at 1 °C).

Substrate cleaning. InP(100) wafer with markers is cleaned with buffered oxide etch (NH_4F:HF = 7:1) (5 min), rinsed with H_2O, IPA (10 min).

Hard mask (1 in Extended Data Fig. 1). Sacrificial layer deposition microwave oxygen plasma (10 min, 200 ml min^{-1}, power 100 W, PVA Tepla 300); PECVD 20 nm SiO_x deposition (300 °C, Oxford Instruments PlasmaLab 80 Plus); oxygen plasma (60 s, power 40 W).

Fabrication of trenches (2–8 in Extended Data Fig. 1). Spin primer (sticking layer) AR 300-80 at 2,000 r.p.m., bake at 180 °C for 2 min; spin resist AR-P 6200.13 at 6,000 r.p.m., bake at 150 °C for 3 min; write trench patterns using EBL (dose 350 μC cm^{-2}); developing in AR 600-546 for 1:30 min in ultrasonic agitation; ultrasonic rinse in IPA for 30 s, blow dry; RIE (reactive ion etch) mask (23 W, 50 standard cubic centimetres (sccm) CHF_3, 2 sccm Ar, Leybold Hereaus, 12 min); wet etch in HCl (37%):H_3PO_4 (85%) ratio 5:1 (15 s, 1 °C); strip the resist in PRS3000 at 88 °C for 20 min; removing hard mask in buffered oxide etch (NH_4F:HF = 7:1) (5 min).

Third, SiO_x is stripped in BHF (5 min) and 20 nm of PECVD Si_xN_y is deposited on the substrate to prevent the parasitic InSb thin film growth which competes with nanowire growth[30]. EBL step followed by a short (40 s) buffered oxide etch (NH_4F:HF = 20:1 + surfactant (Triton)) is used to define openings in the Si_xN_y mask. Metal evaporation (8 nm of Au) and lift-off are used to position Au catalysts (10–50 nm in size) in the openings in the Si_xN_y (Extended Data Fig. 2). Detailed descriptions of the processing steps are presented below.

Deposition of the mask (1 in Extended Data Fig. 2). PECVD 20 nm Si_xN_y deposition (300 °C, Oxford Instrumentals PlasmaLab 80 Plus); oxygen plasma (60 s, power 40 W).

Dots formation (2–8 in Extended Data Fig. 2). Spin primer (sticking layer) AR 300-80 at 2,000 r.p.m., bake at 180 °C for 2 min; spin resist AR-P 6200.04 at 4,000 r.p.m., bake at 150 °C for 3 min; write dot patterns using e-beam lithography (dose 700–800 μC cm^{-2}); developing in AR 600-546 for 1:30 min in ultrasonic agitation; ultrasonic rinse in IPA for 30 s, blow dry; opening the holes in Si_xN_y mask with buffered oxide etch (NH_4F:HF = 20:1) + 5 drops of surfactant Triton X-100 (40–60 s); rinse with H_2O, IPA (10 min); evaporation of 10 nm Au; lift-off in PRS3000 at 88 °C for 2 h; rinse in warm (>50 °C) H_2O; rinse in IPA for 1 min, blow dry.

Nanowire growth. To remove organic residues from the wafer caused by the photoresist layer, O_2 plasma (10 min, 55 sccm O_2, 300 W plasma power) was used before loading into an horizontal Aixtron 200 metal–organic vapour phase epitaxy (MOVPE) reactor with infrared lamp heating. InP nanowires, which act as the mediator for InSb nanowire growth, were grown at 450 °C for 19 min using tri-methyl-indium (TMI), phosphine (PH$_3$) and HCl (1%) with precursor molar fractions X_i(TMI) = 7.6 × 10^{-6} and X_i(PH3) = 9 × 10^{-3} and X_i(HCl) = 8.3 × 10^{-6}. HCl was used to suppress unwanted sidewall growth. InSb nanowires were grown at 495 °C using tri-methyl-indium (TMI) and tri-methyl-antimony (TMSb) with precursor molar fractions X_i(TMI) = 2.8 × 10^{-7} and X_i(TMSb) = 5.1 × 10^{-5}, for 35 min. For both processes, the reactor pressure was 50 mbar, with a total flow of 6,000 sccm and H_2 was used as a carrier gas.

Growth of superconducting aluminium islands. Nanowire networks are transferred *ex situ* to a molecular beam epitaxy (MBE) chamber where an atomic hydrogen clean (20 min under continuous rotation, 380 °C, 5 × 10^{-6} torr H_2 pressure) is first performed to remove the native oxide from the InSb nanowire surface[31]. Subsequently, samples were cooled down to about 120 K by active liquid-nitrogen cooling. Careful alignment of nanowires relative to the Al source is important for well-controlled shadowing of the nanowires. Samples are aligned such that the Al flux is parallel to the long edge of the trenches, as illustrated in Fig. 2a. Al cell temperature was 1,085 °C, resulting in a growth rate of around 2 Å min^{-1}. Immediately after growth, samples were transferred *in situ* to an MBE chamber equipped with an ultrahigh-purity O_2 source where they were dosed with approximately 10^{-5} torr of O_2 for 15 min. This step is important because a so-formed self-terminating oxide layer will 'freeze-in' the Al film, preventing it from diffusing and forming Stranski–Krastanov Al islands, while the sample is being heated up to room temperature in an ultrahigh vacuum, before unloading from the MBE chamber.

Aharonov–Bohm devices. *Device fabrication recipe.*

1. Transfer hashtag nanowires onto a p-doped Si substrate covered by 285 nm SiO_2 layer, serving as a back-gate dielectric.

2. Spinning bi-layer PMMA: first PMMA 495K A6 at 3,000 r.p.m. spinning rate, bake at 175 °C for 10 min. Then PMMA 950K A2 at 2,000 r.p.m., bake at 175 °C for 10 min.

3. Write designed contacts and side gates patterns with e-beam.

4. Develop in developer (MIBK:IPA = 1:3) for 1 min, clean in IPA for 1 min, air-gun blow dry.

5. Remove scum, oxygen plasma 1 min with power 100 W, pressure 1.95 mbar (with Faraday cage in to screen the plasma).

6. Sulfur passivation: dip the chip in ammonium sulfide solution (3 ml (NH_4)$_2$S mixed with 290 mg sulfur powder, then diluted with de-ionized water at a volume ratio of 1:200) at 60 °C for 30 min. Then, rinse the chip in de-ionized water and transfer to an evaporator.

7. Helium milling for 30 s with a Kauffman ion source. Then continue to evaporate 10 nm Cr, followed by 200 nm of Au.

8. Lift off in acetone.

Measurement and analysis. All the four Aharonov–Bohm devices were measured in a He-3 fridge with based temperature of about 300 mK. During the measurement, the side gates (grey in Fig. 3a left inset) were kept grounded, and the global back gate is used to turn on the conducting channels in the hashtag arms. The back gate voltage is 13.35 V for the measurement in Fig. 3a.

Ensemble average of FFT. The FFT spectrum shown in Fig. 3b is an ensemble average of the absolute values of 25 individual FFT spectra[32]. The individual FFTs were calculated from the corresponding magnetoconductance traces (including the one in Fig. 3a), which were measured successively with gate voltage values between 13.3 V and 13.7 V (resulting in conductance values between 0.7 × 2e^2/h and 0.9 × 2e^2/h). A smooth background is subtracted from the original magnetoconductance curves before the FFT is calculated.

Estimation of hashtag loop area. The estimation is based on the SEM images of the device. We took the middle of the wire as the loop boundary to estimate the area, while the error bar of the area is estimated based on the accuracy of the nanowire length we measured from SEM images.

Estimation of phase coherence length. The amplitude of the Aharonov–Bohm oscillations is calculated by integrating the obtained Fourier spectrum over the frequency range corresponding to the expected h/e peak. This amplitude decays as $\Delta G \propto \exp(-L/L_\Phi(T))$, where L is the relevant device length (we took as half of the loop circumference, that is, $L = 1$ μm). L_Φ is the phase coherence length which is a function of temperature. The exponential suppression of ΔG over temperature suggests that L_Φ is proportional to T^{-1}: $L_\Phi(T) = a/T$ (ref. 27). The coefficient a can be extracted from the slope of exponential suppression in Fig. 3d, to be about 0.7 μm K. This allows us to estimate phase coherence length at different temperatures.

Hard-gap devices. InSb nanowire with two shadowed aluminium islands is contacted by Au/Cr. Argon plasma etching was used to remove the aluminium film before evaporation of normal contacts. One normal contact is deposited right next to the shadowed region to replace one aluminium island. The second normal contact is on the other end of the nanowire, sufficiently apart from the shadowed region not to affect the superconducting properties in its vicinity, serving as a current drain for the superconducting contact.

Device fabrication recipe.

1. Transfer InSb–Al nanowires onto a p-doped Si substrate covered by 285 nm SiO_2 layer, serving as a back-gate dielectric.

2. Spinning PMMA 950 K A6 at 4,000 r.p.m., leave the chip in a vacuum chamber pumped with a turbo for overnight.

3. Write designed electrode contact patterns with e-beam, beam dosage: 2,300 μC cm^{-2}, 1,900 μC cm^{-2} and 1,800 μC cm^{-2} for fine, coarse and bonding pads pattern, respectively.

4. Development: (MIBK:IPA = 1:3) for 1 min, IPA for 1 min, blow dry.

5. Ar plasma etch for 4 min (with Ar pressure 3 mTorr, 100 Watts) to etch away Al, AlO_x, InSb surface oxide and part of the InSb nanowires. To prevent the PMMA from burning due to a long plasma etch, one can perform short plasma etch (for example, 20 s) for 12 times with 40 s break between each etch to let the chip to cool down.

6. Evaporate 10 nm Cr, followed by 100 nm of Au.

7. Lift off in acetone.

Measurement and analysis. Devices X (main text), Z and M were measured in a dilution refrigerator with a base temperature of about 20 mK, while device Y was measured in a He-3 fridge with a base temperature of about 300 mK.

Sub-gap versus above-gap conductance fitting in Al–InSb devices. We assume there is a single transmitting channel in the shadow region with transmission T. The above-gap conductance is conductance of normal carriers: $G_N = (2e^2/h) \times T$, while sub-gap conductance, based on Beenakker's formula[28], is: $G_S = (2e^2/h) \times 2T^2/(2-T)^2$. Thus G_S can be plotted as a function of G_N as shown in Fig. 4c (red line). For the experimental data, at each gate voltage, we get the above-gap conductance by averaging the conductance at bias (V) much larger than the gap (Δ), while the sub-gap conductance is obtained by averaging a small bias window at zero bias.

Contact transparency estimation based on Andreev enhancement. In Extended Data Fig. 8b, we obtain Andreev enhancement for sub-gap conductance reaching

$1.7 \times 2e^2/h$. Based on Beenakker's formula, setting this value equal to G_S, we can extract a transparency $T \approx 0.96$.

Data availability. The main data that support the findings of this study are available within the paper. Additional data are available from the corresponding author on request.
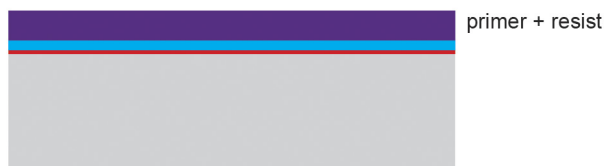
29. Adachi, S. & Kawaguchi, H. Chemical etching characteristics of (001) InP. *J. Electrochem. Soc.* **128,** 1342–1349 (1981).
30. Dalacu, D. *et al.* Selective-area vapour–liquid–solid growth of InP nanowires. *Nanotechnology* **20,** 395602 (2009).
31. Webb, J. L. *et al.* Electrical and surface properties of InAs/InSb nanowires cleaned by atomic hydrogen. *Nano Lett.* **15,** 4865–4875 (2015).
32. Meijer, F. E. *et al.* Statistical significance of the fine structure in the frequency spectrum of Aharonov–Bohm conductance oscillations. *Phys. Rev. B* **69,** 035308 (2004).
33. White, L. K. Bilayer taper etching of field oxides and passivation layers. *J. Electrochem. Soc.* **127,** 2687–2693 (1980).
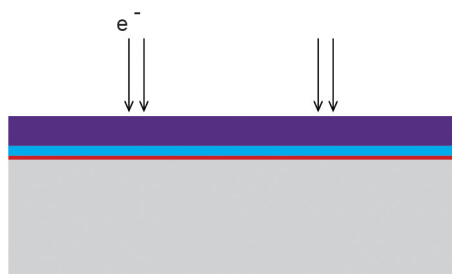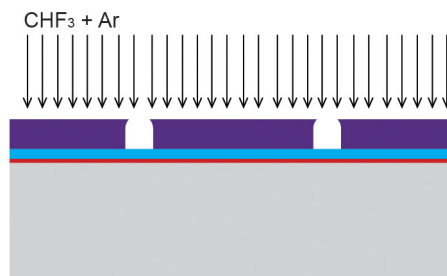
1.

SiO$_x$
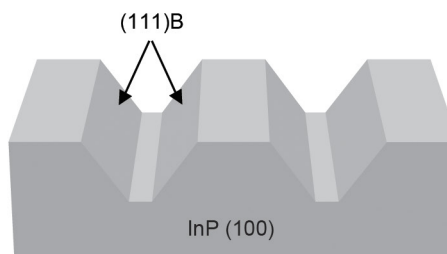InPO$_x$

InP (100)

2.

primer + resist

3.

e$^-$

4.

5.

CHF$_3$ + Ar

6.

7.


54.7$^{\mathrm{o}}$

8.

(111)B

InP (100)

**Extended Data Figure 1 | Fabrication of InP substrate with trenches.**
1–8: Schematic illustration of the processing steps. **1**, An out of the box wafer is etched in 7:1 buffered HF; an oxygen plasma step is performed to create a 'sacrificial' native oxide layer of 1.9 ± 0.1 nm (ref. 33); a 20 nm SiO$_x$ hard mask is deposited followed by another oxygen plasma treatment. **2, 3, 4,** The electron-beam primer and resist layer is spun; rectangular windows of $\sim$200 nm are written using EBL and subsequently developed. **5, 6,** The hard mask is etched using reactive ion etching (RIE) with CHF$_3$ and Ar. **7, 8,** The wet etch in HCl (37%):H$_3$PO$_4$ (85%) with 5:1 ratio is performed to expose (111)B facets in InP (100) and the hard mask is removed using 7:1 buffered HF. A detailed fabrication recipe can be found in Methods.
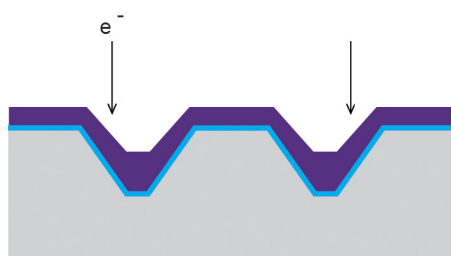
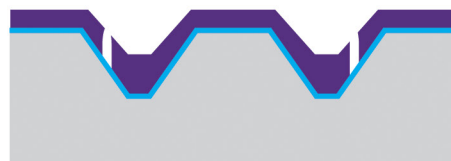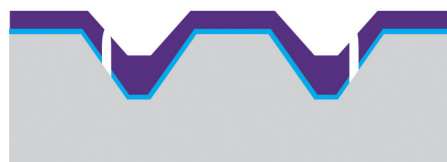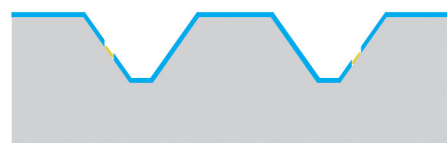**1.**
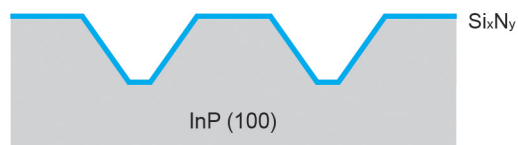
2.
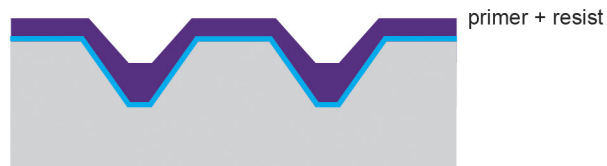
3.

4.

5.

6.

7.

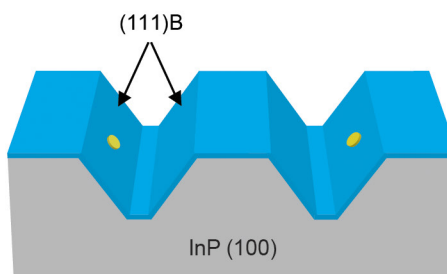**8.**

Extended Data Figure 2 | Catalyst deposition. 1–8: Schematic illustration of the processing steps. **1,** 20 nm Si_xN_y mask is deposited followed by an oxygen plasma treatment. **2–4,** E-beam primer and resist layer is spun (nominal resist thickness needs to be half of the depth of the trenches); arrays of dots (10–50 nm) are written on inclined (111)B facets using e-beam lithography and the resist is then developed. **5,** Openings in Si_xN_y mask are defined using short 20:1 buffered HF etch. **6–8,** 10 nm of gold is evaporated through the opening in Si_xN_y mask followed by a lift-off. A detailed fabrication recipe can be found in Methods.

a

b
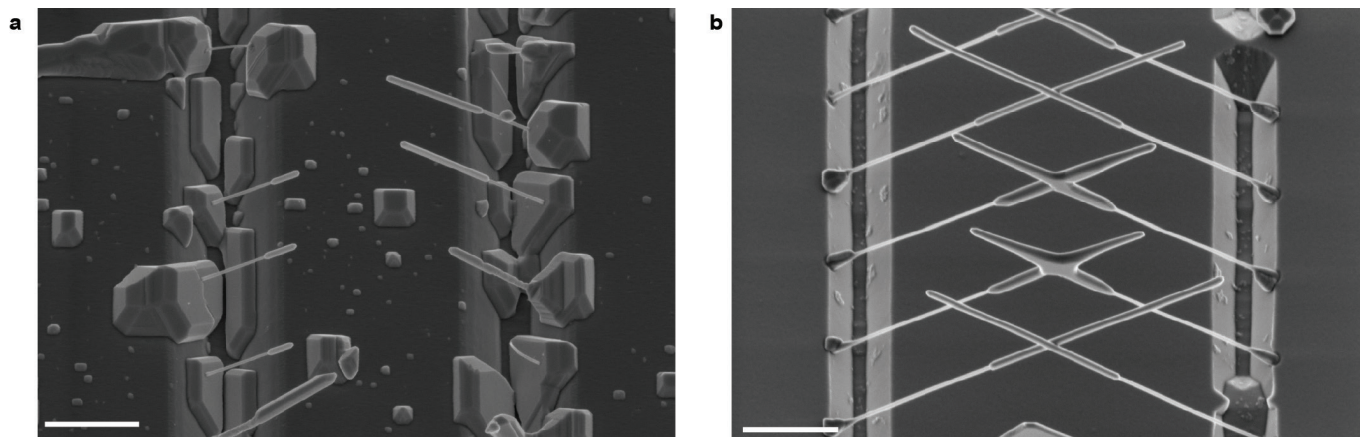
Extended Data Figure 3 | Role of the Si$_x$N$_y$ mask in InSb nanowire growth. a, b, A 30°-tilted SEM image of InP–InSb nanowires grown on a substrate without (**a**) and with (**b**) Si$_x$N$_y$ mask. A substantial amount of parasitic thin film growth is observed in **a**. Concave edges of the trenches act as a preferential nucleation site for InSb growth. Thin-film InSb growth is in direct competition with InSb nanowire growth, resulting in short nanowires and a very low yield of crossed junctions. By covering the substrate with a Si$_x$N$_y$ mask, the growth is restricted to areas where the InP substrate is exposed[30]. This, in combination with approximately 100 times lower molar fractions of TMIn and TMSb used for the growth of wires shown in **b**, eliminates the unwanted InSb layer growth and allows for growth of high-aspect-ratio InSb nanowires which merge into networks. Both scale bars are 1 μm.

a

b
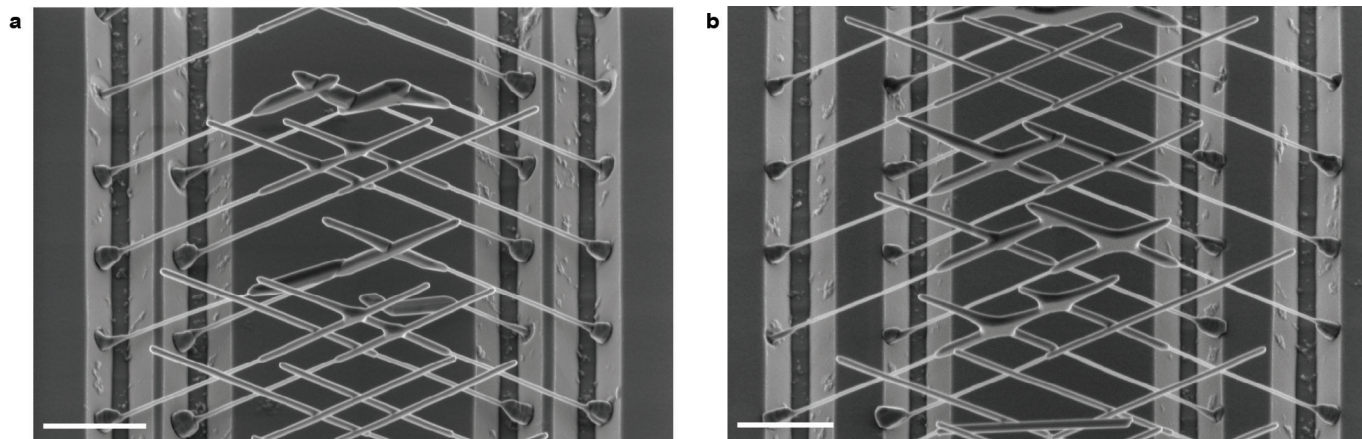
Extended Data Figure 4 | Lithographic control over the trench design layout enables growth of hashtags spanning different loop areas. **a**, **b**, InSb nanowire networks grown on trenches with different spacing between the left–left (L_1, L_2) and right–right (R_1, R_2) trenches, labelled a and b in Fig. 1a, respectively. Control over the dimensions of the trenches allows us to tune the length of the hashtag parallelogram. The scale bars are 1 μm.
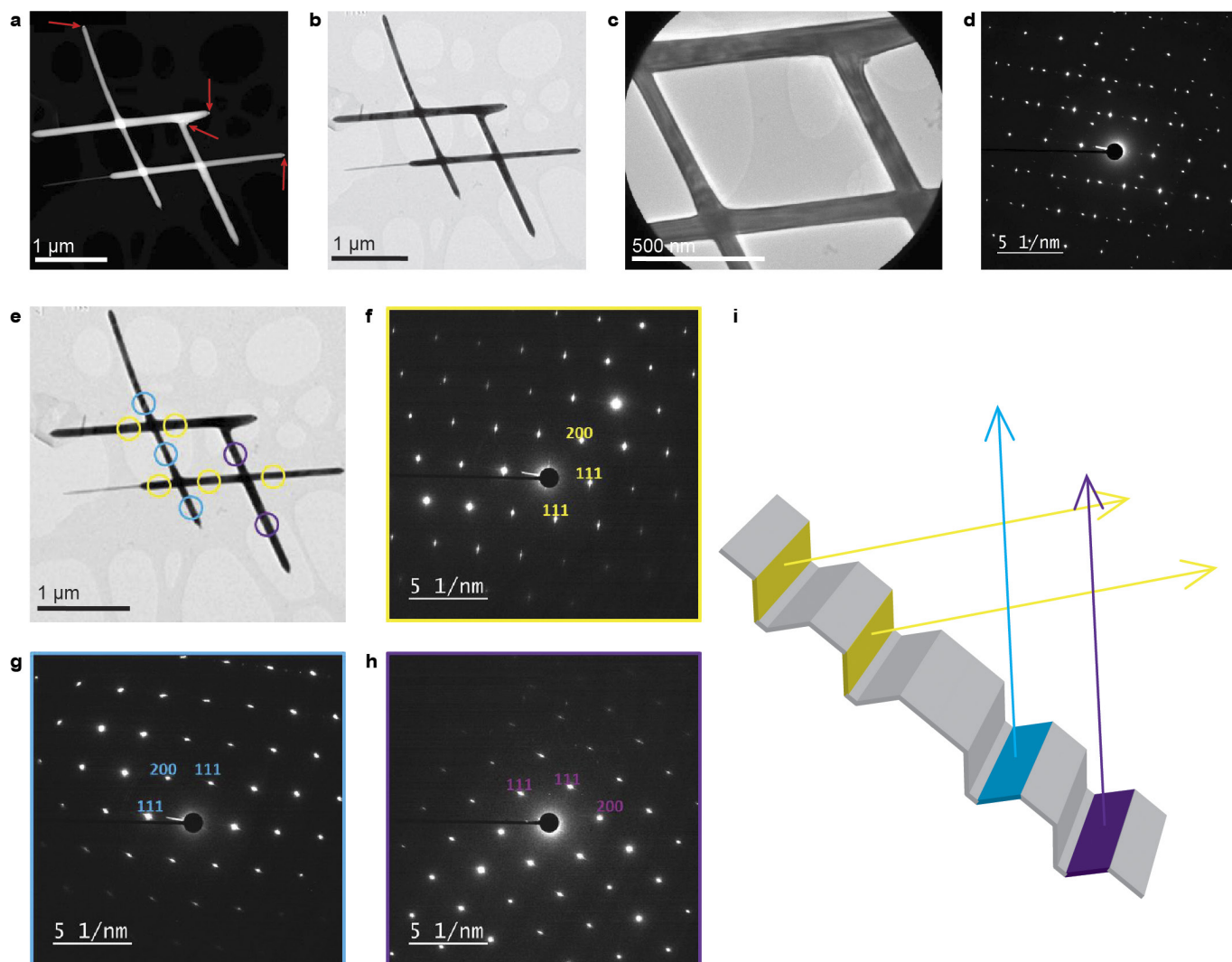
Extended Data Figure 5 | Structural analysis of a hashtag taken from the substrate and deposited on a holey carbon film using a micromanipulator in the SEM. a, High-angle annular dark field (HAADF) scanning TEM image of the hashtag. The red arrows indicate the positions of the gold catalyst particles. For one wire, the InP stem is present and recognizable. **b**, Corresponding bright field (BF) TEM image. **c**, BFTEM image displaying the central part of the hashtag as well as the 1.3 μm aperture inserted for the selected area electron diffraction (SAED) pattern displayed in **d**. The pattern represents a superposition of three twin-related ⟨110⟩ zone axis patterns. **e**, To reveal the orientation of the individual wires of the hashtag, SAED patterns for all the wires were acquired, using a smaller SAED aperture diameter of 0.25 μm. Three different ⟨110⟩ zone axis patterns were recorded. The colour coding of the apertures in **e** corresponds to the SAED patterns in **f**–**h**. **i**, Schematic representation of the formation of the hashtag presented in the TEM images. The blue and purple nanowires have two different orientations, related by a 180° rotation around their long axis. Thus, one of the wires has the same orientation as the substrate wafer, while the other one is twin related. The two yellow wires have identical orientations that differ from the orientations of the two other wires. Thus, these yellow wires are also twin-related to the substrate, though their rotation axis is different from that of the blue and purple wires.
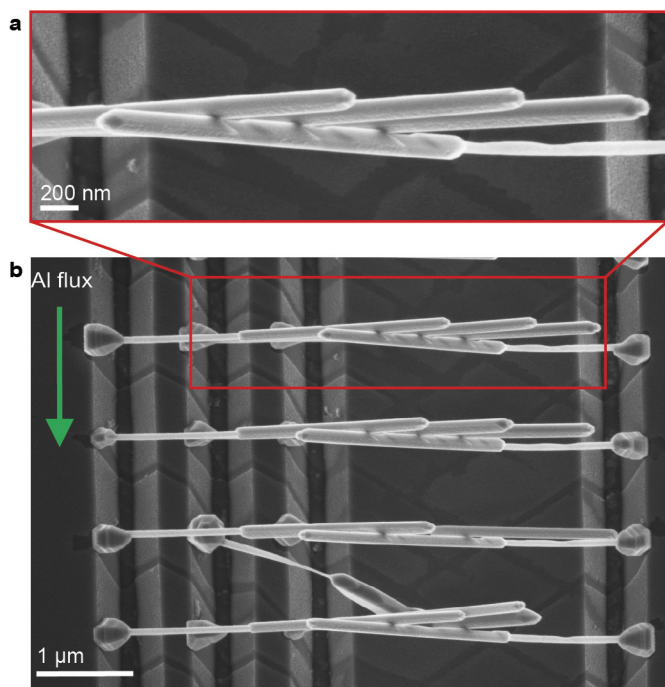
Extended Data Figure 6 | The number of superconducting islands, $n + 1$, is determined by the number of wires, n, directly in front of the shadowed nanowire. a, A high-magnification top-down SEM image of the region indicated by a red rectangle in **b**. The three nanowires facing the Al flux cast shadows on the wire directly behind them, resulting in InSb nanowires with four superconducting islands. The shadowing offset is about 200 nm. The nanowires bend towards each other owing to the e-beam exposure during imaging.
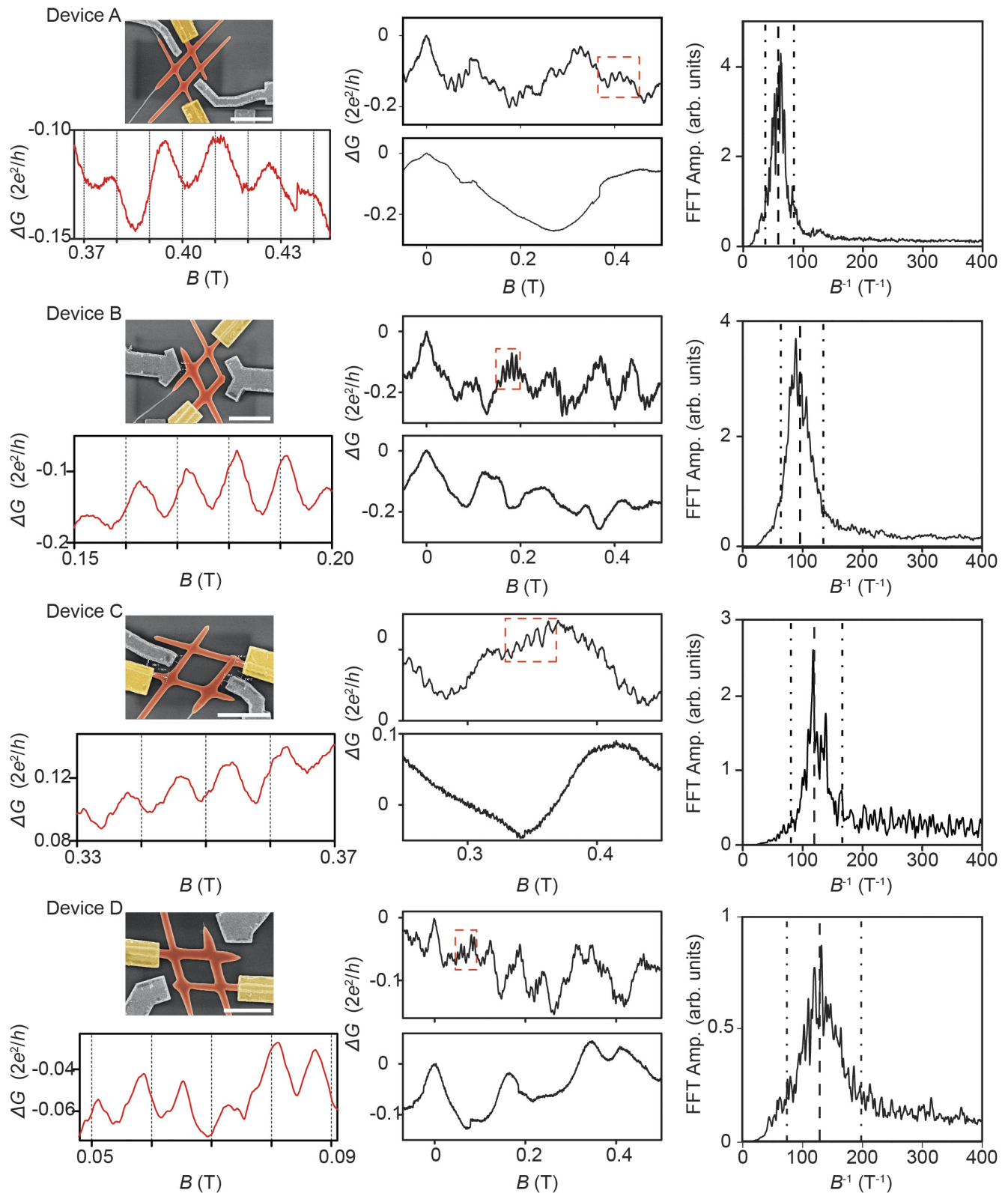
Extended Data Figure 7 | Aharonov–Bohm oscillations in four devices with different hashtag surface areas. Device A has been studied in detail in the main text. For all devices, left upper panel shows the pseudo-coloured SEM image of the device, middle panels show the conductance measured in the out-of-plane (top) and in-plane (bottom) magnetic field and right panel shows the ensemble averaged FFT spectrum. Only the out-of-plane magnetic field, whose flux penetrates through the hashtag loop, gives Aharonov–Bohm oscillations which indicates that the Aharonov–Bohm oscillations indeed originate from the coherent interference of electron waves of the two separated conducting nanowire arms. A magnified view of the Aharonov–Bohm oscillations (a zoom-in on the region indicated by an orange rectangle in the upper middle panel) is shown in the lower left panel, while the right panel shows the averaged FFT spectrum. Plot of the peak frequency, assigned from the averaged FFT spectra, as a function of the measured loop area of the four devices is shown in the inset of Fig. 3b. Weak-antilocalization peak at $B = 0$ T is present for both field directions, and in three (A, B, D) out of four devices, suggesting the strong spin–orbit nature of the InSb nanowire network. The corresponding back gate voltages of the four devices are: 15 V, 9 V, 12 V and 9 V, respectively. Temperature is 300 mK. The scale bar is 1 μm.
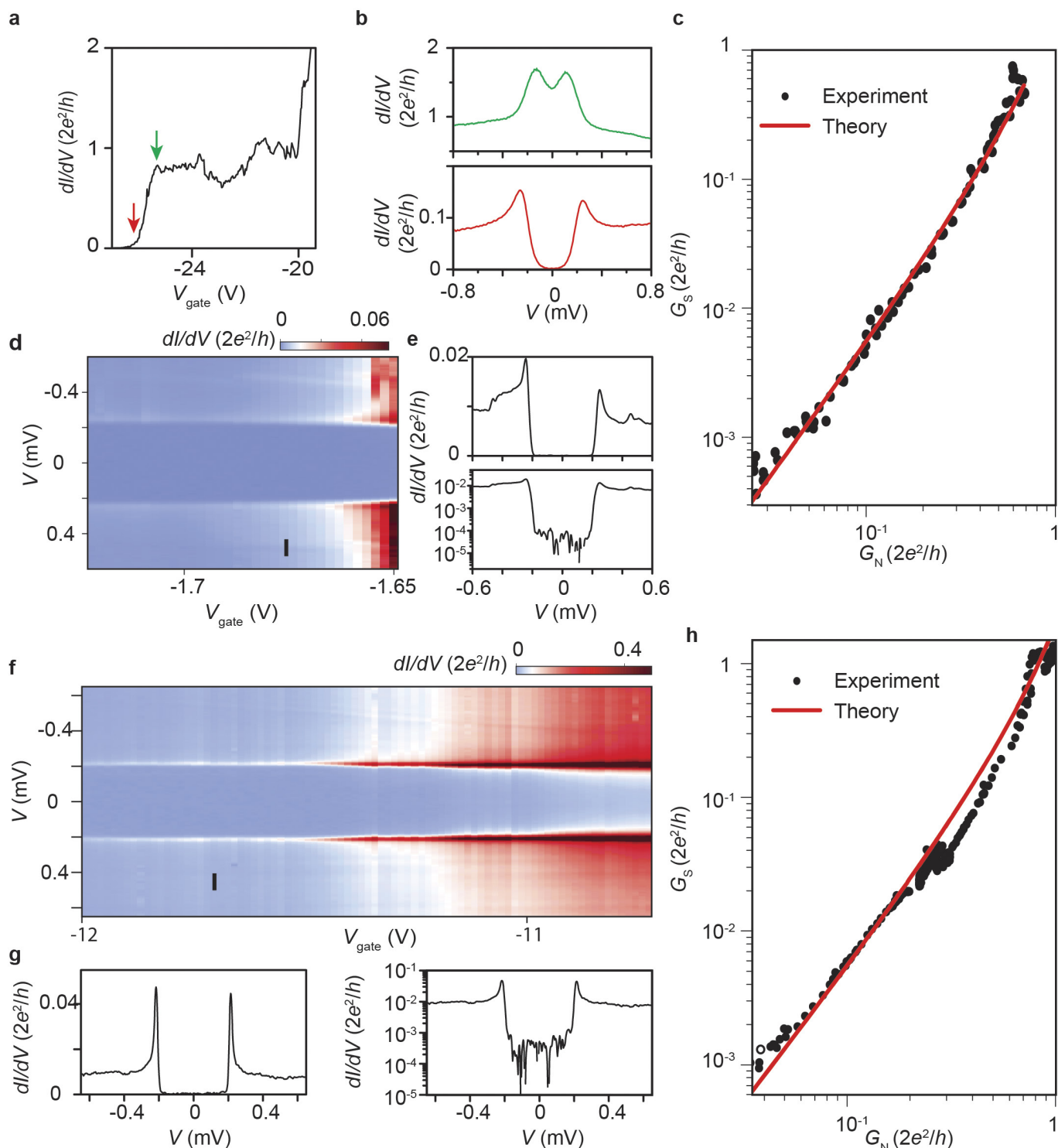
Extended Data Figure 8 | Ballistic transport, Andreev enhancement and hard gap in additional Al–InSb devices. a, Above-gap (normal carriers) conductance of device Y as a function of V_{gate}. A conductance plateau near the quantized value ($2e^2/h$) can clearly be seen, indicating ballistic transport. **b**, dI/dV versus bias voltage in the open and tunnelling regime, resolving strong Andreev enhancement (green) and a hard gap (red), respectively, with V_{gate} indicated by arrows in panel **a**. The coherence peaks are smeared out owing to thermal broadening (temperature of about 300 mK for this device). The Andreev enhancement is due to Andreev reflection: an incoming electron reflects as a hole at the N–S interface generating a Cooper pair. This process effectively doubles the transported charge from e to $2e$, enhancing the sub-gap conductance. Our enhancement factor reaches $1.7 \times 2e^2/h$, indicating the high Al–InSb

interface transparency, with transmission larger than 0.96. The small dip in Andreev enhancement near zero bias is due to mode mixing induced by minimal residual disorder[11]. **c**, Sub-gap versus above-gap conductance of device Y (black dots), and a theoretical fit (red) based on the Beenakker formula, showing perfect agreement over three orders of magnitude conductance change. **d**, dI/dV of device Z as a function of V_{gate}. **e**, A line cut from panel **d** (black bar), plotted in linear (top) and logarithmic scale (bottom). The above-gap/sub-gap ratio is larger than 300. **f**, dI/dV of device M as a function of V_{gate}. **g**, A line cut from panel **f** (black bar), plotted on linear (left) and logarithmic scale (right). **h**, Sub-gap versus above-gap conductance of device M (black dots), and the Beenakker theoretical fit (red). Device shown in the main text (X), and devices Z and M are measured at around 20 mK.