

Capacitance spectroscopy of gate-defined electronic lattices

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(Dated: 27 September 2017)

Semiconductors form an enticing platform for the realization of quantum lattice physics, as conduction band electrons allow for electrostatic confinement, readout and control while undergoing an interplay of gauge fields, band physics and electron-electron interactions. This combination offers the potential to realize a wide host of quantum phases. So far, attempts at measuring artificial lattices of confined electrons in semiconductors, whether optically or in transport, were limited by disorder in the material as well as by inhomogeneities induced by the fabrication. Capacitance spectroscopy provides a technique that allows for the direct measurement of two-dimensional electron systems and enables to reduce effective disorder. Here we present a measurement and fabrication scheme that builds on capacitance spectroscopy and aims at imposing a periodic potential modulation on a two-dimensional electron gas. We characterize disorder levels and (in)homogeneity and develop and optimize different gating strategies at length scales where interactions are expected to be strong. A continuation of these ideas might see to fruition the emulation of interaction-driven Mott transitions or Hofstadter butterfly physics.

Artificial lattice structures have the potential for realizing a host of distinct quantum phases¹. Of these, the inherent length scale of optical platforms allows for a clean emulation of quantum mechanical band physics, but also means interactions are weak and going beyond a single-particle picture is difficult^{2,3}. For electronic implementations in solid-state, interactions can be made non-perturbatively strong, potentially leading to a host of emergent phenomena. An example is shown in graphene superlattices, where not only Hofstadter's butterfly physics⁴⁻⁷ but also interaction-driven and emergent fractional quantum Hall states in the butterfly appear⁸. The ideal platform would host a designer lattice with tunable electron density and lattice strength, allowing to emulate band physics for a wide variety of lattice types and giving access to the strong-interaction limit of correlated Mott phases⁹⁻¹³. Semiconductor heterostructures with nano-fabricated gate structures provide this flexibility in lattice design and operation, yet inherent disorder in the host materials as well as the short length scales required make the realization of clean lattices difficult¹⁴⁻¹⁶.

In this Letter, we demonstrate a novel experimental platform for realizing artificial gate-induced lattices in semiconductors, based on a capacitance spectroscopy technique, with the potential to observe both single-particle band structure physics such as Hofstadter's butterfly and the interaction driven Mott insulator transition. We characterize disorder levels and develop and optimize different gating strategies for imprinting a two-dimensional periodic potential at length scales where in-

teractions are expected to be strong.

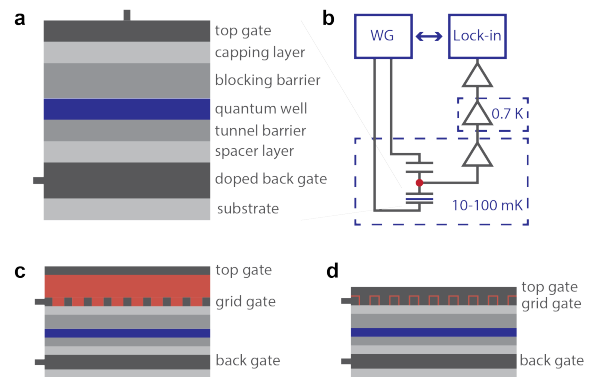


FIG. 1. (a) Capacitance spectroscopy layer stack. Apart from the top gate(s), all layers are GaAs/Al_xGa_{1-x}As, grown by molecular-beam epitaxy. (b) Bridge set-up for equilibrium capacitance measurements, where the amplitude ratio and phase difference between measurement signals on the sample and a reference capacitor created by a waveform generator (WG) are set to impose a constant zero voltage at the bridge point (red dot), which is amplified at different stages and read out using a lock-in amplifier. (c)-(d) Different two-layer gate designs to impose a periodic potential on the 2DEG. Dielectric spacer is depicted in red.

In our capacitance spectroscopy set-up¹⁷⁻¹⁹, a doped back gate region is tunnel coupled to a two-dimensional electron gas (2DEG) above, whose density of states (DOS) modifies the capacitance between the back gate and a metallic top gate (see Fig 1a). At the limits of zero or infinite DOS, the system behaves like a simple parallel plate capacitor, described by the distance between top gate and back gate or top gate and quantum well, re-

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spectively. The capacitance is read out using a bridge design with a reference capacitor, where the voltage at the bridge point is kept constant (Fig 1b) by changing the amplitude ratio and phase difference of AC signals applied to each capacitor (see SupA for experimental details). To impose a periodic potential in the 2DEG, we pattern the metallic gate into a grid shape and add a second non-patterned top gate on top of the grid gate. From a capacitance spectroscopy perspective, this double-gate structure can be made with two different designs. In the first design, the second (top) gate is separated from the other gate by a thick dielectric layer, rendering its capacitance to the other (grid) gate negligible. If so, we can ignore the second gate from an AC perspective altogether (Fig 1c). Alternatively, we can minimize the separation between the two gate layers, such that the capacitance between the two top gates exceeds the sample capacitance. As seen in AC, the two gates then effectively form a single gate (Fig 1d).

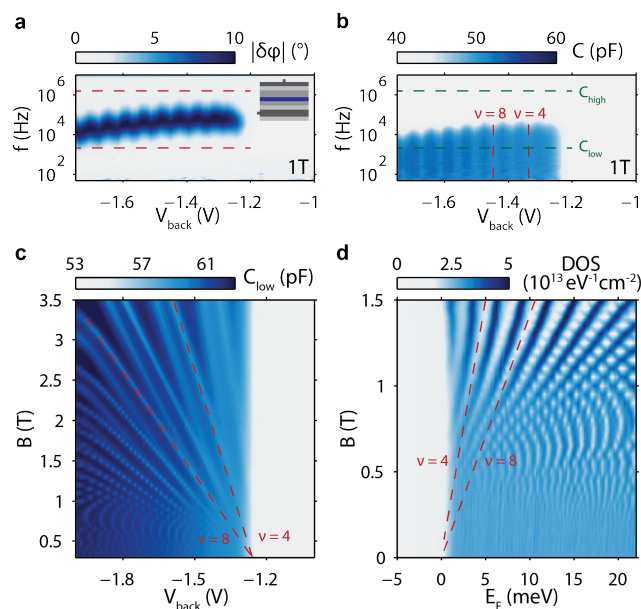


FIG. 2. (a) Bridge equilibrium phase as function of back gate voltage and measurement frequency. (b) Global gate capacitance as function of bias voltage and measurement frequency. (c) Landau fan diagram: device capacitance as function of bias voltage and magnetic field, showing onset of accumulation, integer quantum Hall levels and exchange splitting. (d) Charge addition spectrum derived from the low field regime of (c), allowing us to assess disorder from Landau level visibility. The gaps at filling factors $\nu = 4$ and $\nu = 8$ are indicated. At lower fields, the small Landau level spacing leads to aliasing in the image.

In order to assess disorder levels, we first measure devices with a single uniform top gate. We measure the capacitance at frequencies below and above the rate at which electrons tunnel between the 2DEG and the doped back gate region as a function of bias voltage and magnetic field. Having measured the capacitance at low

and high frequencies, we calculate the equilibrium DOS. There are essentially two unknown parameters in this conversion, namely the distance from top to bottom gate and the relative location of the 2DEG itself. The former can be directly inferred from the capacitance at high frequency, the latter by using either the known effective mass or the Landau level splitting with magnetic field as benchmarks (see SupB for details on this conversion).

As a magnetic field is turned on, we see the onset of Landau level formation. For larger magnetic fields, the exchange enhanced Zeeman splitting becomes visible as well, indicating the non-perturbative effect of the Coulomb interaction on increasingly confined electrons (Fig 2c). We focus on the low-field data (Fig 2d) and infer disorder levels from the density of states data (Fig 2e). Gaussian fits to the Landau levels yield typical widths ranging between 0.4-1 meV at densities above 10^{11} cm^{-2} . The Landau levels themselves (aliased at low fields in in Fig 2d) become visible above fields of roughly 0.25 T, corresponding to densities per Landau level of $1.2 \times 10^{10} \text{ cm}^{-2}$ and cyclotron gaps of 0.43 meV. The Landau level width did not depend on small changes in temperature or excitation voltage and was consistent across fabrication schemes, but did vary with the wafer used. Therefore, we consider it a heuristic metric for the achievable disorder levels on a particular wafer. We have tried to optimize wafer design to minimize this disorder, whilst allowing for the imposition of a periodic potential. All in all, over twenty different wafers were measured (see SupC for considerations and an overview of used heterostructure designs). Whereas changing layer thicknesses was found to have only a little effect, decreasing (increasing) the Al content in the tunnel (blocking) barrier led to substantial reductions in measured disorder levels.

We next fabricate devices with grid and top gates based on both designs of Fig 1c-d to assess the imparted periodic potential. Square grid metallic gates are fabricated at pitches of 100-200 nm using electron beam lithography and evaporation in a standard lift-off process (Fig 3a-b). In the first design, both gates are made of Ti/Au(Pd) and separated by $> 200 \text{ nm}$ layer of oxide, such as plasma-enhanced chemical vapor deposition grown SiO_x or plasma-enhanced atomic layer deposition grown AlO_x . The top gates are electrically isolated from one another, with a stray capacitance between them of several pF typically. In the second design, both gates are made of Al, and an oxygen (remote) plasma oxidation step is used after depositing the first step to ensure sufficient electrical isolation between the two layers. In this design, we measure resistances exceeding $1 \text{ G}\Omega$ over several V and capacitances of several hundred pF between the two metallic layers (see SupD for a description of different designs and fabrication details).

The strength of the imparted periodic potential depends both on the gate design and on the maximum voltages that can be applied. These maximum voltage differences arise for instance because of the onset of leakage through the heterostructure or the accumulation of

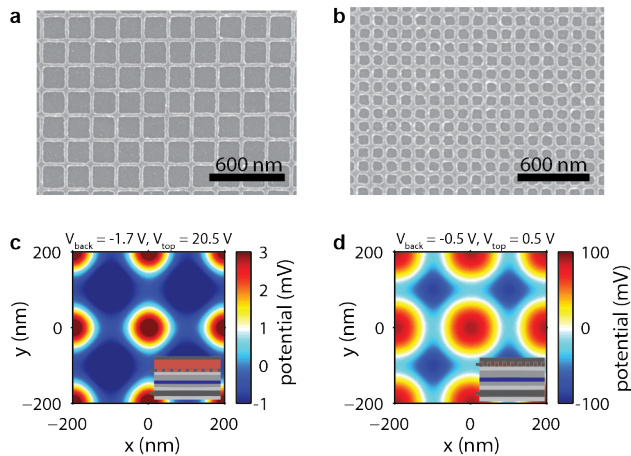


FIG. 3. (a)-(b) Electron micrograph of a 200 nm periodic 20 nm Al grid gate layer. (b) Similar, for a 100 nm periodic gate layer. (c)-(d) Electrostatic simulations of imparted potential in the 2DEG in both designs, with a 200 nm periodic 20 nm wide square grid gate, and using denoted gate voltages. For (c), we use a 350 nm SiO₂ dielectric and flat top gate. For (d), we use a 5 nm spacer dielectric separating the two top gates. Voltages used are roughly half of the empirical maximum voltage we can set for both designs, $V_{\text{grid}} = -0.5$ V for both. The thin-dielectric design clearly allows for imposing a stronger periodic potential.

charges in the capping layer, and as such depend on heterostructure details, such as Al concentration and layer thicknesses. Electrostatic simulations indicate that, as is to be expected, significantly larger top gate voltages are required in the first design as compared to the second one, in order to achieve a sizable periodic potential in the 2DEG (Fig 3c-d). Furthermore, we note that the screening induced by mobile charges in the back gate region has both a positive and a negative effect. To understand this, we recognize that the screening of potential modulations is length dependent. On the positive side, disorder in the heterostructure as well as imperfections in the fabrication represent the shortest length scales and as such are screened the most strongly. On the negative side, electron-electron interactions and the imposed potential modulation itself are screened as well, and more so as the lattice dimension is reduced.

For measurements of two-layer gate devices of both designs (Fig 4), we keep the grid gate potential fixed, given that it serves as the gate voltage of the first transistor in the amplification chain, and map out the remaining two gates over as large a range as possible. Initial devices of both designs indeed show accumulation as function of the two gate voltages. The direction perpendicular to the onset of accumulation indicates homogeneous filling of the 2DEG, whereas the periodic potential modulation builds up in the direction parallel to the onset of accumulation. At voltages where we expect a flat periodic potential, and for our final set of devices, we can still distinguish well-defined Landau levels, indicating that

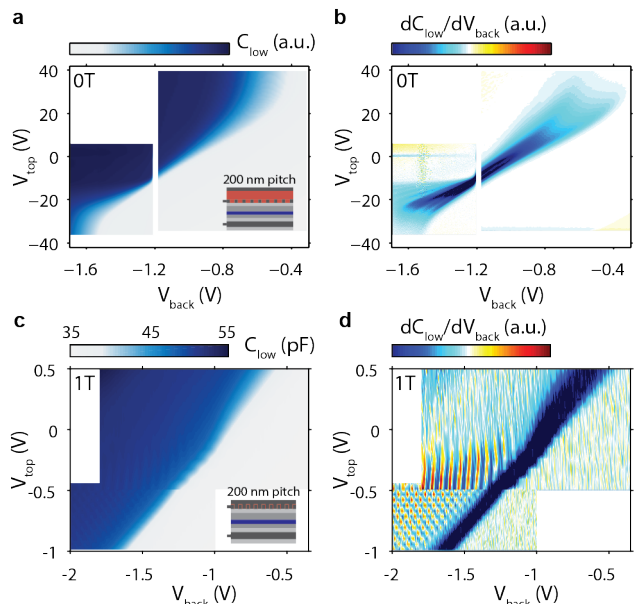


FIG. 4. (a) Capacitance as function of back gate and top gate voltages for a device with a 200 nm periodic square grid gate and a 360 nm SiO₂ dielectric separating the two gate layers (see inset and Fig. 3a). (b) Derivative of capacitance data. (c)-(d) Similar data taken for a device with aluminum overlapping gates (see inset) at 1 T. No clear effect is seen on the onset of accumulation, although at finite field we see that as the top gate voltage is made more positive than the grid gate voltage, Landau levels (aliased in topgate voltage) get blurred out.

the added fabrication steps themselves do not severely increase the disorder levels (Sup D). For the first gate design, we find a saturation to the effect of the top gate in gating the 2DEG at gate voltages exceeding 20 V in absolute value. This could be a sign of charges building up at the capping layer to dielectric interface or in the dielectric itself that screen the top gate, and limits the potential we can impose on the 2DEG. For the second gate design, a maximum voltage difference of roughly 2 V can be set between the back gate and the surface gates before leakage starts to occur.

Using either gate design we find both gates to influence the accumulation of charges in the quantum well as expected, but neither shows clear evidence of a lattice potential imposed on the 2DEG (Fig 4). At zero magnetic field, a lattice potential would lead to minibands that manifest as periodic modulations in the density of states (and capacitance) with a period corresponding to two electrons per lattice site, or 5×10^9 cm⁻² for a 200 nm square grid. Expressed in mV on the backgate, this corresponds to a period of 6 mV. At finite magnetic field, Landau levels are expected to show structure due to Hofstadter butterfly physics^{15,20}, with the largest gaps expected around $k \pm 1/4$ of a flux quantum Φ_0 threading each lattice plaquette (with k an integer; this corresponds to $52k \pm 13$ mT for a 200 nm grid). Furthermore, a strong

enough periodic potential would allow interaction effects to dominate. Miniband gaps split as filling starts to occur with a period of one electron per lattice site, akin to the interaction-driven Mott transition¹¹. These effects are not seen yet, however, as we run detailed scans in the relevant sections of measurements such as those shown in Fig 4. We therefore discuss next whether the imposed lattice potential exceeds the disorder levels, whether the induced density modulations can be resolved, and whether the lattice potential from the grid gate itself is sufficiently homogeneous.

For devices of the first design, the onset of accumulation broadens both at negative and positive top gate voltages (Fig 4a-b), indicating that the 200 nm periodic potential exceeds disorder levels (0.4-1 meV) at low densities, as expected based on electrostatic simulations of the strength of the imposed potential (Fig 3). There is an inherent asymmetry between positive and negative top gate values for the first design, possibly because effective disorder levels are smaller when charges accumulate mainly underneath the grid gate, as compared to when charges accumulate mainly underneath the dielectric. Although the widening of the onset of accumulation is less pronounced for the second design, the effect of gating is seen at finite fields, at which a voltage difference between the grid and top gate effectively blurs out the gaps between Landau levels (Fig 4c-d), showing that the imposed local potential must be comparable to or stronger than the Landau level spacing at 1 T (1.7 meV). We conclude that also for the second design, the 200 nm periodic potential exceeds disorder levels.

If we compare the $5 \times 10^9 \text{ cm}^{-2}$ density modulations expected from miniband formation with the $1.2 \times 10^{10} \text{ cm}^{-2}$ broadening of low-field Landau levels (global gate devices at high densities, i.e. this is a lower limit on disorder), it is not surprising that gaps are not yet seen opening up at densities corresponding to the filling of (pairs of) electrons on each lattice site. This suggests that either lattice size or wafer disorder has to be further reduced. As it proves hard to lift off plaquettes of metal that are smaller than roughly 40 nm by 40 nm, there is not much room to reduce lattice dimension further in this particular fabrication scheme (Fig 5a). For 100 nm pitch grids, the period of the density modulations is expected to be four times larger, but would still be comparable to current best-case scenario Landau level broadening. As such, reducing intrinsic disorder seems the way forward. An appropriate goal would be to make double layer gate devices with distinguishable Landau levels at fields below 200 mT.

The visibility of Hofstadter butterfly gaps depends not only on the intrinsic disorder in the device, but also on any inhomogeneity in the plaquette sizes, as this would entail a different number of flux quanta threading through different plaquettes. If the size variations from electron micrographs of our devices translated to identical size variations in the periodic potential (Fig 5b), we should just be able to distinguish the largest gaps¹⁵. It is hard to assess, however, whether this indicator from the

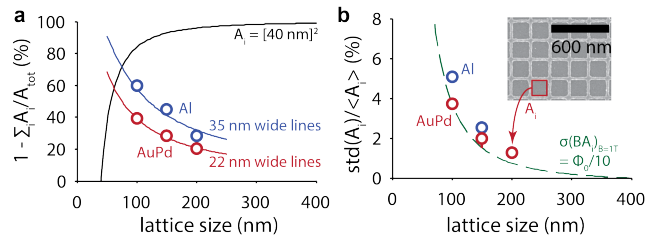


FIG. 5. (a) Fraction of surface area covered by the grid gate as function of lattice size. Black line indicates a grid with the smallest possible plaquettes allowed by the lift-off process, whereas the blue (red) line indicates the surface covered by a grid with metallic lines of 35 nm (22 nm). (b) Variation in relative area of non-metal plaquettes in the grid gate layer (A_i , see inset) as function of lattice size, as a measure of fabrication (in)homogeneity. The green dashed line indicates variations in plaquette area that coincide with variations of a tenth of a flux quantum at 1 T. Blue (red) points indicate grid gates made of Al (AuPd) for both figures.

electron micrographs directly correlates to the relevant physics in the 2DEG.

There is room for further optimization of our devices. On the heterostructure side, the distance between the back gate and the 2DEG can be further increased, compensating with a decreased Al content in the tunnel barrier to keep the tunnel rate fixed. Furthermore, part of the spacer layer can be grown at reduced temperatures, which has been shown to strongly reduce disorder by limiting the diffusing of Si dopants from the back gate region²¹. On the fabrication side, there is still room left for a modest reduction of the lattice periodicity with the current lift-off process. Even smaller length scales can be obtained by switching to dry etching of the grid pattern, albeit at an unknown impact to wafer disorder levels.

In summary, we have demonstrated a novel platform intended for the realization of artificial lattices of interacting particles. Although fine tuning the design to the point where a sufficiently homogeneous and strong periodic potential can be applied remains to be done, the quantum Hall data already shows how the strong-interaction, low-temperature limit can be reached. Such a platform has potential for studying the interaction-driven Mott insulator transition^{11,22} and Hofstadter butterfly physics⁴ with finite interactions, and can be extended from the steady-state measurements presented here to include time-domain measurements of excited states²³.

ACKNOWLEDGMENTS

The authors acknowledge useful discussions with O.E. Dial, R.C. Ashoori, G.A. Steele, R. Schmits, A.J. Storm and the members of the Delft spin qubit team as well as experimental assistance from M. Ammerlaan, J. Haanstra, S. Visser and R. Roeleveld. This work is supported by the Netherlands Organization of Scientific Research (NWO) VICI program, the European Commission via the integrated project SIQS and the Swiss National Science Foundation. The work at Purdue was supported by the US Department of Energy, Office of Basic Energy Sciences, under Award number DE-SC0006671. Additional support from the W. M. Keck Foundation and Microsoft Station Q is gratefully acknowledged.

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Supplementary Information for Capacitance spectroscopy of gate-defined electronic lattices

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A. Capacitance bridge

The capacitance bridge is built on a printed circuit board (PCB) that is mounted on the 10 mK mixing chamber stage of a dilution fridge and whose main components are the device, the reference capacitor and a high electron mobility transistor (HEMT, that serves as the first amplifier). By mounting the HEMT orthogonal to the PCB surface, we can apply magnetic fields to the sample without influencing the amplification chain. All D/C lines on the sample PCB have R/C filters on top of the filtering in the fridge. A 10 and 40 M Ω resistance is used to bias the bridge point and top gate in D/C, respectively, and a bias-tee is added to bias the back gate on top of the measurement signal. The high frequency lines are not attenuated in the fridge, as we found this to lead to ground loop issues, but are instead attenuated on the PCB itself. Measurement excitations are simple sinusoidal signals that get attenuated to the V level and are generated using a signal generator at room temperature. The bridge point voltage is amplified further at 0.7 K and at room temperature and measured using a lock-in.

An iterative scheme is implemented to minimize the bridge point voltage by updating the amplitude ratio and phase difference of the two excitations as gate voltages and applied magnetic field are changed. The excitation on the sample side is kept constant and the excitation on the reference capacitor side is updated based on the secant method. For this, we model the bridge as a linear system of complex variables: $Y = AX + B$, where X is the reference signal, Y is the output from the lock-in, and A and B are complex numbers. Given two iterations with reference signals X_i and X_{i+1} and respective output values Y_i and Y_{i+1} , A and B are calculated as well as $X_{i+2} = -B/A$, which is subsequently set and Y_{i+2} measured. As the first two iterations, we take the last set reference signal as well as a point with a typically 1 % higher amplitude and a tenth of a degree increased phase. Convergence is reached when the amplitude dif-

ference between the last two reference signals drops below some pre-defined value, typically chosen to be several parts per thousand of the amplitude itself. The sample capacitance C_{sample} follows from the reference capacitor value C_{ref} and the applied amplitude ratio $R = \frac{V_{\text{ref}}}{V_{\text{sample}}}$ and phase difference $\delta\phi = \pi + \phi_{\text{ref}} - \phi_{\text{sample}}$ at equilibrium: $C_{\text{sample}} = \cos(\delta\phi)RC_{\text{ref}}$.

B. Conversion from capacitance to density of states

In calculating density of states from capacitance data, we follow a procedure described before¹⁷. As a start, $C_{\text{high/low}}$ are measured as function of gate voltages and magnetic field values (Fig 2b and Fig S 2a). Note that the heterostructure stack is designed to keep the tunnel frequency in the middle of the experimental measurement window (Fig 2a-b): below 1 kHz signal to noise ratio declines (mainly because of the $1/f$ noise of the first transistor in the amplification chain) and above 2 MHz systematic errors occur (we find asymmetric cross-talk between the two excitation signals and the second transistor in the amplification chain). We model the system as a parallel plate capacitor made up of the top and bottom gates, with the potential for added charges at the location of the quantum well, as sketched in Fig S 1:

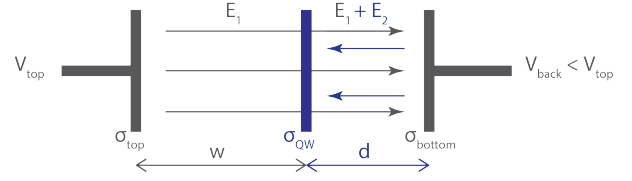


Figure S 1. Schematic representation of the device as a parallel plate capacitor of distance $w + d$ with an inserted quantum well at a distance d from the back gate. When the DOS at the quantum well is nonzero, charges can build up.

The total voltage difference over the device is a combination of the electric fields $V = V_{\text{back}} - V_{\text{top}} = E_1(w + d) + E_2d$, which in turn depends on the charges on the plates as $V = \frac{\sigma_{\text{top}}(w+d)}{\epsilon} + \frac{\sigma_{\text{QW}}d}{\epsilon}$. The total capacitance, which is the one measured at low enough frequencies, is defined as $C_{\text{low}} = \frac{\partial Q}{\partial V} = A \frac{\partial \sigma_{\text{top}}}{\partial V} = \frac{\epsilon A}{w+d} - \frac{dA}{w+d} \frac{\partial \sigma_{\text{QW}}}{\partial V} +$ small terms that depend on changing distances and which we ignore. The first term describes the bare capacitor, and is therefore equal to the total capacitance measured at high frequencies: $C_{\text{high}} = \frac{\epsilon A}{w+d}$. The second term is the one of interest. It describes changes between the capacitance measured at low and high frequency because of the addition of charges in the quantum well, which allows us to infer changes in electron density using $\frac{\partial n}{\partial V} = -\frac{1}{e} \frac{\partial \sigma_{\text{QW}}}{\partial V} = \frac{1}{eA} \frac{w+d}{d} (C_{\text{low}} - C_{\text{high}})$ (Fig S 2b).

The voltage required to change the Fermi level E_F of the quantum well can be found using a similar deduction to the one described above, and is described by

a voltage-dependent lever arm $\alpha \equiv -e \frac{\partial V}{\partial E_F}$. We find the lever arm by following the dependence of the Fermi level in the quantum well through changes in the electric field as $\frac{\partial E_F}{\partial V} = -ew \frac{\partial E_1}{\partial V} = -e \left(\frac{w}{w+d} + \frac{e}{\epsilon} \frac{wd}{w+d} \frac{\partial n}{\partial V} \right)$ (Fig S 2c). The first term describes how the Fermi level of a gapped system in the quantum well ($\delta n = 0$) changes with bias as expected given its relative location $\frac{w}{w+d}$ between the plates of a simple parallel plate capacitor (Fig S 2c). It is the second term that encompasses the electron filling, showing the lever arm to increase when charges can be added to the quantum well (after accumulation this becomes the dominant term, see Fig S 2b). Given the above expressions for density and Fermi level changes as function of gate voltage, we can define the density of states in the 2DEG through $DOS = \frac{\partial n}{\partial V} \frac{\partial V}{\partial E_F} = \frac{1}{e^2 A} \frac{w+d}{d} \alpha (C_{\text{low}} - C_{\text{high}})$ (Fig S 2d).

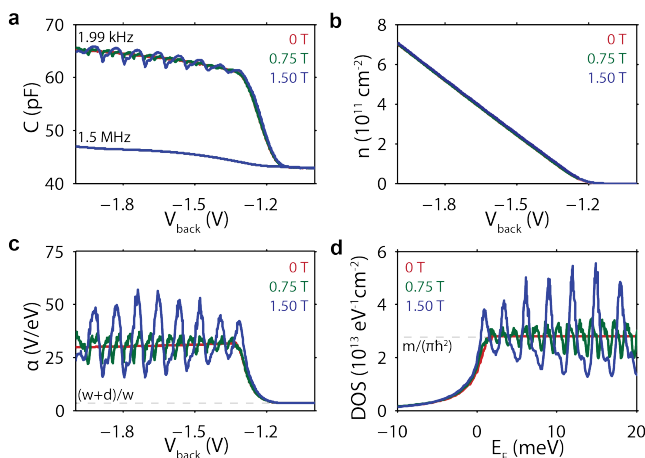


Figure S 2. (a) Capacitance as function of back gate bias at 0 T (red), 0.75 T (green) and 1.50 T (blue), both below and above the tunnel frequency. Top gate is kept constant for all measurements as it serves as the bridge point, which is also directly contacted to the gate of the first transistor in the amplification chain. (b) Density as function of back gate bias. As the system becomes more gapped between Landau levels at higher fields, steps start to form in the graph that indicate the filling of distinct levels at well-defined densities. (c) Lever arm as function of back gate bias. Note that the quantum capacitance of a large density of states in the 2DEG increases the voltage required to change the Fermi level, as expected. At zero density of states, however, the lever arm is simply the geometric ratio expected from the relative location of the quantum well between the top and bottom gate. (d) Density of states as function of the Fermi energy, which is the integrated lever arm. We choose zero in energy to lie close to accumulation.

As indicated by changes in C_{high} in Fig S 2a, the distances describing the system are non-static with gate voltage. In the case of $(w+d)$, this is most likely due to back gate charges populating part of the spacer layer as the electric fields bend the conduction band edge, indeed increasing C_{high} for more negative back gate voltages. The exact location of the charges in the quantum well

and related distance d , however, we cannot directly infer from an independent measurement. As a first guess, the growth distances combined with the $(w+d)$ extracted from C_{high} suffices. A better estimate can be made using the known linear degeneracy of Landau levels with magnetic field, $n_{\text{LL}} = \frac{2eB}{h}$ (Fig S 2b). To obtain the best possible calibration, however, we compensate for any further dependence of the relative quantum well position on back gate voltage by pegging the 0 T DOS after accumulation to the expected value of $\frac{m}{\pi \hbar^2} \approx 2.8 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$ (Fig S 2d), and use this calibration for nonzero magnetic field values.

C. Heterostructure details

All in all, over twenty different GaAs/ $\text{Al}_x\text{Ga}_{1-x}$ As wafers grown by molecular beam epitaxy have been used. Here, we present the main considerations and corresponding changes in wafer design that were implemented over the course of this work. In general, we have experimented with varying the design to complement the fabrication (see Sup D) in minimizing the measured disorder and increasing the ability to apply a periodic potential, either through reduced screening of top gates or through the increase of the leakage voltages, allowing for larger top gate voltages to be used. Growth details of wafers referred to below can be found in Table S I.

The initial wafer (W1) design was based on Dial²³, and was grown on a conducting substrate. This simplifies the fabrication of single-gate devices, as an unpatterned ohmic back gate contact can be directly evaporated on the back side of the wafer, while simple metallic pads fabricated on the front side can be directly bonded to and used as a top gate. A double-gate design requires dedicated bond pads, which would give a sizable contribution to the total capacitance when fabricated directly on the wafer. The device used for Fig 4a-b in the main text, fabricated on one (W2) of the first round of wafers, therefore, had bond pads on top of the thick dielectric separating the two gates (Fig S 3a). Not only would this not be compatible with the second design, where there is no thick dielectric layer, but we also found bonding yield to be very low due to poor adhesion of the dielectric layers on the GaAs surface. Furthermore, handling both sides of a substrate during fabrication risks contaminating the front surface, and is particularly suboptimal when detailed features (grid gates) are present as well.

Subsequent wafers were therefore grown with a 400-800 nm thin degenerately Si doped back gate region that is contacted from the front side of the wafer, and is etched to form electrically isolated device and bond pad mesas (Fig S 4a and Fig S 5a). In first attempts at reducing disorder levels and allowing for the setting of stronger periodic potentials, quantum well width (15 and 30 nm) and spacer layer thickness (25 and 35 nm) were varied.

In further attempts to optimize the trade-off between periodic potential that can be set at a fixed voltage and

the maximum voltage we can apply to the gates before leakage kicks in, we varied the blocking barrier thickness (40, 50, 60 and 70 nm) as well as fabricated devices with a thin dielectric layer (see wafers M1, W3 and Sup D) added underneath the gates. None of these, however, managed to increase the maximum potential we could impose on the 2DEG, or decrease disorder levels noticeably.

As an alternative to varying layer thickness, differing the aluminum concentration between the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ blocking and tunnel barrier (from $x = 0.31$ everywhere to $x = 0.36$ in the blocking barrier and $x = 0.20$ in the tunnel barrier) did allow for a sizable increase in Landau level sharpness, with the results of Fig 2 and Fig 4c-f fabricated on wafer M2.

D. Design and fabrication details

Several different designs and fabrication recipes were used throughout this work to fabricate devices with two layers of gates: a grid gate and a uniform global gate on top. All devices measured have an area of $200\ \mu\text{m}$ by $200\ \mu\text{m}$. First we describe these different designs briefly, their differences and limitations. Next we give some general information on steps that have been employed for many of these fabrication runs. Lastly, we provide the detailed information for a fabrication run of the second design with overlapping aluminum gates, which serves as a clear example from which the steps required for fabricating the other devices measured can be easily deduced.

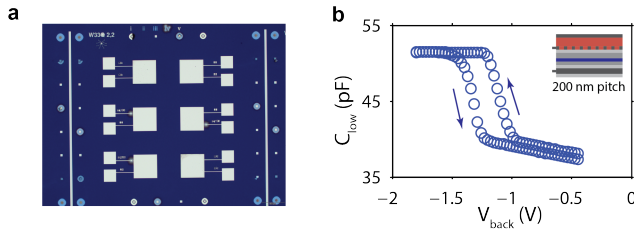


Figure S 3. (a) Optical image of a device cell of the first design with a 366 nm thick AlO_x dielectric layer. Top left and bottom right squares are ohmic contacts, which could have also been fabricated on the back side of the wafer. The other squares are three double-gate devices and one single-gate device, each with two bond pads. Contacting the grid layer underneath the dielectric is done using etched vias. (b) Capacitance as a function of back gate for a device from (a), showing hysteresis as function of either top or back gate voltage (shown).

The first design, with a thick dielectric separating the two gate layers, has been fabricated with two different dielectrics. For the results of Fig 4a-b, plasma-enhanced chemical vapor deposition (PECVD) of 360 nm of SiO_2 as dielectric was used, which was found to give noisy devices. We have also fabricated devices with 366 nm of plasma-enhanced atomic layer deposition (ALD) grown

AlO_x dielectric. Although these devices were less noisy, they showed large top gate hysteresis, rendering them practically impossible to measure with (Fig S 3b). Furthermore, etching small vias through such a thick layer of alumina is very cumbersome. All devices of the first design had low yield in bonding because of poor adhesion of the dielectric layers to the GaAs surface.

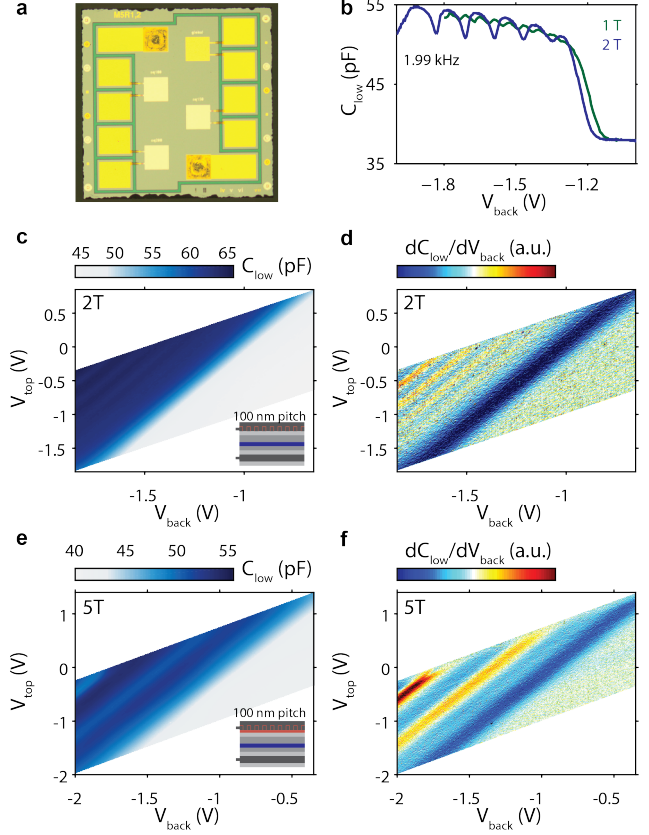


Figure S 4. (a) Optical image of a device cell containing two ohmic contacts at top left and bottom right as well as a single-gate device on the top right and three double-gate devices. The dielectric-filled etched region that separates the device mesa from the bonding pads is visible in green. (b) Landau level cuts at 1 and 2 T of the overlapping aluminum double gate layer device of Fig 4c-f in the main text. (c)-(d) Capacitance and derivative at 2 T as a function of back gate and top gate voltages for initial devices with Al overlapping gates at a 100 nm pitch. (e)-(f) Data for a similar device at 5 T, but with a 5 nm AlO_x dielectric placed underneath the grid gate.

Our first results of the second design were obtained with a 5 nm ALD grown AlO_x dielectric separating a Ti/Au grid and top gate layer. These devices were found to show hysteresis similar to Fig S 3b as well as phase offsets close to accumulation. In parallel, we worked on devices with overlapping aluminum gates (Fig S 4a), where the oxidation of the initial layer serves as the spacer between the grid and the top gate. Landau level signature on the capacitance is still clear for these double gate

Table S I. Heterostructure details.

	W1	W2	M1	W3	M2
capping layer	GaAs	GaAs	GaAs	GaAs	GaAs
	10 nm	10 nm	5 nm	10 nm	5 nm
blocking barrier (Al content)	0.316	0.316	0.316	0.315	0.360
	60 nm	60 nm	40 nm	60 nm	60 nm
quantum well	GaAs	GaAs	GaAs	GaAs	GaAs
	23 nm	23 nm	23 nm	23 nm	23 nm
tunnel barrier (Al content)	0.316	0.316	0.316	0.315	0.199
	13 nm	13 nm	14 nm	14 nm	16 nm
spacer layer	GaAs	GaAs	GaAs	GaAs	GaAs
	25 nm	15 nm	15 nm	15 nm	15 nm
back gate	GaAs n ⁺⁺	GaAs n ⁺⁺	GaAs n ⁺⁺	GaAs n ⁺⁺	GaAs n ⁺⁺
	800 nm	800 nm	400 nm	400 nm	400 nm
tunneling frequency at 0T, $n \approx 10^{11} \text{ cm}^{-2}$	1 MHz	200 kHz	2 kHz	30 kHz	100 kHz
lowest field at which Landau levels can be distinguished	3 T (at 4 K)	0.65 T	0.50 T	0.40 T	0.25 T
comments	n ⁺⁺ doped wafer	n ⁺⁺ doped wafer			

devices, indicating that the disorder is not strongly enhanced by the added fabrication steps (Fig S 4b). These devices initially showed (almost) no signs of imposing a periodic potential (Fig S 4c-d). As an attempt at being able to apply larger gate voltages before leakage through the heterostructure occurs, we have tried the same fabrication but with an additional 5 nm ALD-grown AlO_x dielectric placed underneath the grid gate. However, we found the onset of charges in the capping layer to occur at the same voltages as where leakage occurs for devices without the added dielectric underneath the grid gate, and as such for such a design to yield no increase in the maximum voltage we could apply (Fig S 4e-f). The results of Fig 4c-f in the main text were obtained on overlapping aluminum gate devices without an added dielectric underneath, and on a more optimized wafer (M2).

All lithography steps were performed using electron beam lithography (Vistec EBPG 5000+ or 5200) at 100kV acceleration voltage. Etching $\text{Al}_x\text{Ga}_{1-x}\text{As}$ was done using diluted Piranha (1:8:240 $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$) yielding etch rates of roughly 4 nm/s. Actual etch rate decreases at a timescale of minutes as the H_2O_2 concentration slowly decreases. Etching SiO_2 and AlO_x was done using buffered HF (BOE 1:10) solutions. After either type of wet etch, devices are rinsed repeatedly in H_2O . Adhesion issues for resists with HF etch times longer than 20 s mean iterative etching and re-baking is necessary. For the 366 nm AlO_x layers, this meant we had to use a dry Cl etch to etch the bulk of the depth of the vias before finishing with a wet etch. Metallic layers were deposited using electron-beam evaporation at room temperature and subsequent lift-off in solvent, as detailed below. A single cell is designed to host two

ohmic contacts, three double-gate devices and one single-gate device (Fig S 2a), all of which are 200 μm by 200 μm . Spinning is done at 500 rpm for 5 seconds and 55 seconds at speeds listed below. Note that the lift-off based fabrication of grids allows for different lattices to be made also. As examples, see Fig S 5b-c. An overview of the fabrication steps for realizing double-layer gate devices with aluminum gates is given below. See Fig S 4a for the top view of a finished device and Fig S 5a for schematic side views of the process.

- Ohmic contacts - spin PMMA 495K A8 resist at 6000 rpm - bake 15 min at 175 °C (400 nm) - lithography - development 60 s in 1:3 MIBK/IPA - wet etch of 180 nm in diluted Piranha - evaporation of 5/150/25 nm Ni/AuGe/Ni - lift-off in acetone and IPA rinse - anneal 60 s at 440 °C in forming gas.
- Mesa etch - spin PMMA 495K A8 resist at 6000 rpm - bake 15 min at 175 °C (400 nm) - lithography - development 60 s in 1:3 MIBK/IPA - wet etch of 700 nm in diluted Piranha - sputtering 700 nm of SiO_2 - lift-off in acetone and IPA rinse.
- Bridges - spin PMMA 495K A8 resist at 6000 rpm - bake 15 min at 175 °C (400 nm) - lithography - cross-link PMMA strips through electron beam overdose at 25 mC/cm². These sections act as bridges over which the leads will connect sample mesa and bond pad regions.
- Connection pads and markers - spin PMMA 495K A8 resist at 6000 rpm - bake 15 min at 175 °C (400 nm) - lithography - development 60 s in 1:3

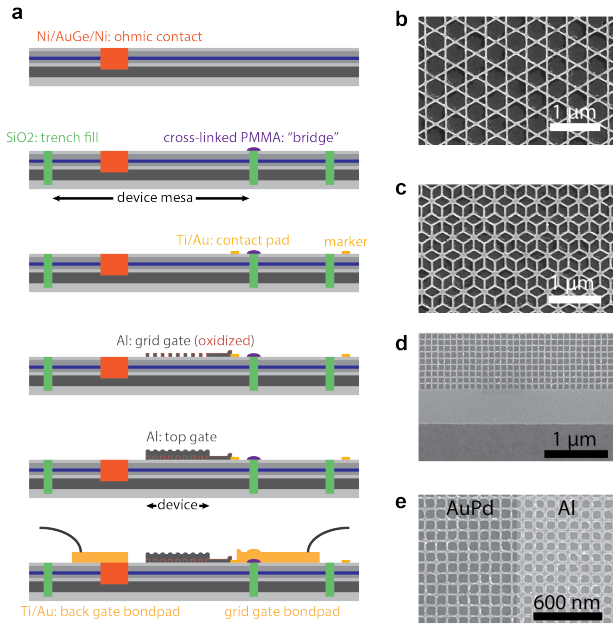


Figure S 5. (a) Overview of the fabrication process. See Fig. S 4a for a top view. Note that the top gate bondpad is not shown in this view, and that the mesa and bridge steps are shown added to the same figure. (b) Electron micrograph of a kagome-type lattice fabricated using the same lift-off recipe as used for the square grids, with 5/15 nm Ti/Au. Note that for non-square lattice such as this, a different lattice is imposed on the 2DEG depending on the polarity of the voltage difference between the grid and top gate. (c) Electron micrograph of a 5/15 nm Ti/Au dice-type lattice gate. (d) Electron micrograph at the edge of a square 100 nm grid, showing the overdosed 'frame' that is used to counter proximity effect induced inhomogeneity effects at the edge of the grid. (e) Electron micrograph of a 100 nm periodic 5/15 nm thick Ti/AuPd square grid (left) and a similar 20 nm thick Al grid (right). Reduced grain size make AuPd detailed structures easier to fabricate.

MIBK/IPA - evaporation of 10/50 nm Ti/Au - lift-off in acetone and IPA rinse. These sections act either as markers or as pads that will be contacted on the top both by the Al gates and the leads contacting the bond pads. We found these thin layers

of metal to be the most robust way to make an electrical connection (typically several Ohm) between the Al gates and the Au bond pads.

- Grid gate - spin CSAR 62.04 resist at 5000 rpm - bake 3 min at 150 °C (72 nm) - lithography - development 70 s pentylacetat and 60 s 1:1 MIBK:IPA - evaporation of 20 nm Al - lift-off in NMP at 70 °C using soft ultrasound excitation for 4 hrs and subsequent acetone and IPA rinse - oxidation in 20 min at 200 °C at 100 mTorr and 300 W RF power using the remote plasma of an ALD machine. We have optimized the lithographic sequential writing such that a 200 μm x 200 μm grid is written in one go and at under a minute, getting rid of stitching errors completely and reducing the effect of drift (typically several tens of nm/min). We have done this by direct programming of an iterative sequence that the e-beam follows in writing the grid instead of the standard procedure of converting a design file (in this case a large square grid) to an e-beam lithography file using BEAMER software. Furthermore, we add a 200 nm thin frame around the grids whose overdose is chosen to counter proximity edge effects (Fig S 5d). Note also that we found the opposite requirements of high resolution and undercut required for lift-off to be best served using a single layer CSAR62 resist. Finally, we find feature size, yield and reproducibility to be limited by the grain size of the evaporated Al, instead of the resist mask or lithography process and contrary to what might be expected. As such, Ti/Au but especially Ti/AuPd gates were easier to fabricate (Fig S 5e).
- Top gate - spin PMMA 495K A8 resist at 6000 rpm - bake 15 min at 175 °C (400 nm) - lithography - development 60 s in 1:3 MIBK/IPA - evaporation of 50 nm Al - lift-off in acetone and IPA rinse.
- Bonding pads - spin OEER-1000 (200cp) lift-off resist at 3500nm - bake 30 min at 175 °C (500 nm) - spin PMMA 950K A2 resist at 2000 rpm - bake 10 min at 175 °C (90 nm) - lithography - evaporation of 50/200 nm Ti/Au - lift-off in acetone and IPA rinse.